

Compal Confidential

Model Name : Q3ZMC

File Name : LA-8481P

# Compal Confidential

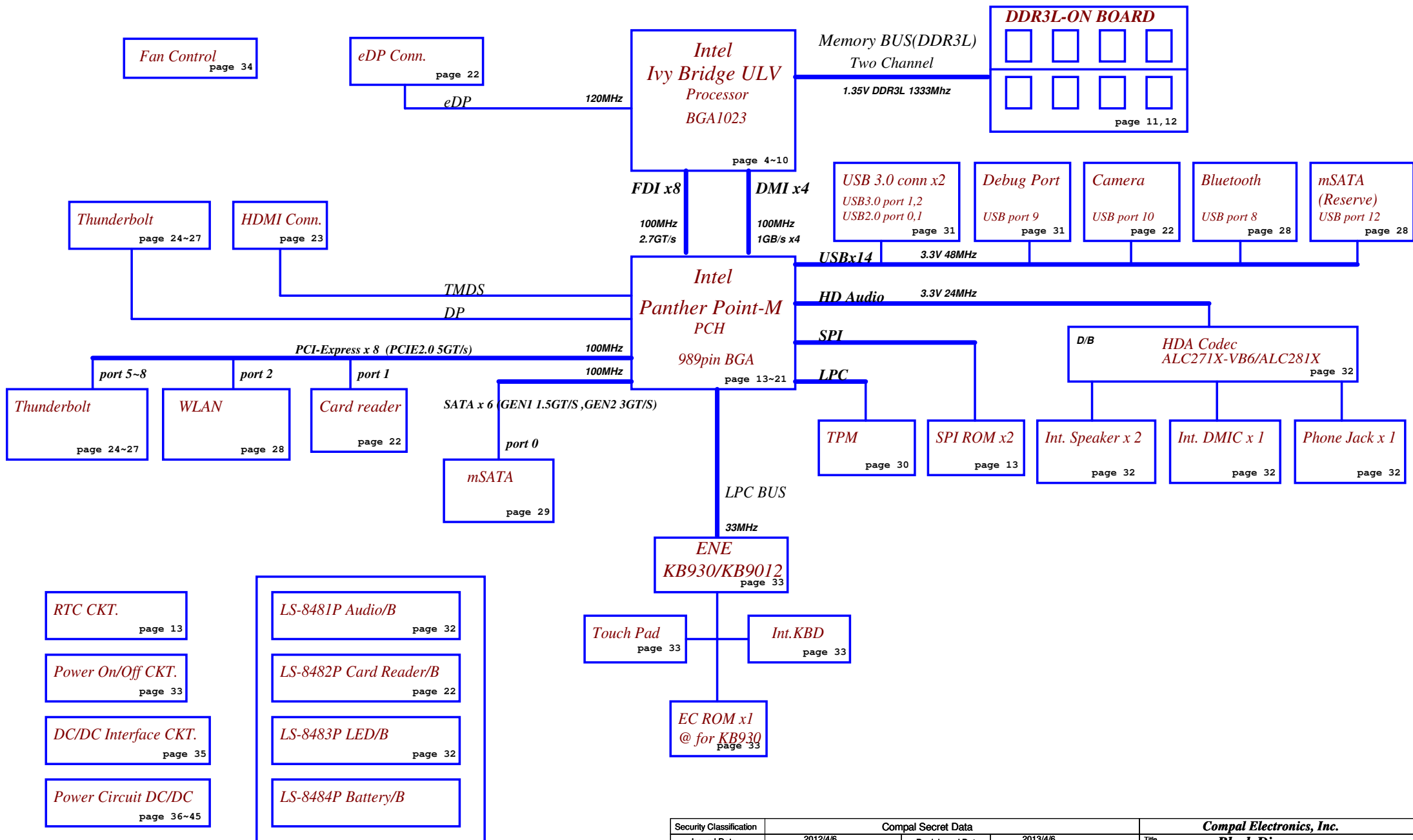
## Q3ZMC UMA M/B Schematics Document

Intel Ivy/Sandy Bridge SFF BGA 1023p Processor  
/Panther Point 989p PCH  
/ DDR3L Memory Down \*8

2012-04-11

REV : 1 . 0 (MP SMT)

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	Cover Page
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				Q3ZMC M/B LA-8481P Schematic	1.0
				Date: Thursday, April 12, 2012	Sheet 1 of 51



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	Block Diagrams	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Q3ZMC M/B LA-8481P Schematic	Rev 1.0
				Date:	Thursday, April 12, 2012	Sheet 2 of 51

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.35V	+1.35VP to +1.35V power rail for DDR3L	ON	ON	OFF
+1.35VS	+1.35V to +1.35VS switched power rail	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR3L terminator	ON	OFF	OFF
+1.5VS	+1.5VSP to +1.5VS power rail for PCH	ON	OFF	OFF
+1.8VS	+3VALW to 1.8VS switched power rail for PCH	ON	OFF	OFF
+3VALW	+3VALWP to +3VALW always on power rail	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Resistor)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW always on power rail	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
ChannelA	A0 1010 000X
ChannelB	A4 1010 010X

BOM Config  
4319HNBOL01:UMA@/DDR3L@/eDP@/USB3.0@/9012@/TB@/IVB@/HM77@/DS3@/TXM@/TPM@/128@/  
4319HNBOL02:UMA@/DDR3L@/eDP@/USB3.0@/9012@/TB@/IVB@/HM77@/DS3@/TXM@/TPM@

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.10.2
1	0.3 DVT:unknown MCU+MKS Motor,With TB IC
2	0.4 PVT1:PADAUK MCU+MKS Motor,Without TB IC
3	0.4 PVT2:PADAUK MCU+MKS Motor,With TB IC
4	1.0
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
UMA	UMA@
CPU	IVB@
PCH	HM77@
DDR3	DDR3@
DDR3L	DDR3L@
On Board DRAM	X76@
128bit RAM	128@
eDP	eDP@
LVDS	LVDS@
USB2.0 Conn	USB2.0@
USB3.0 Conn	USB3.0@
Thunderbolt	TB@
KB930	930@
KB9012	9012@
Normal S3	S3@
Deep S3	DS3@
TPM+TCM	TXM@
TPM	TPM@
TCM	TCM@

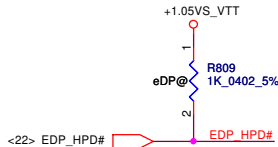
USB Port Table

USB 2.0	USB 1.1	Port	2 External USB Port
EHCI1	UHCI0	0	USB port (Rear side 3.0)
		1	USB port (Rear side 3.0)
		2	
	UHCI1	3	
		4	
		5	
EHCI2	UHCI2	6	
		7	
		8	
	UHCI3	9	Debug Port
		10	Camera
		11	
	UHCI4	12	mSATA(Reserve)
		13	BlueTooth

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Notes List	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number <b>Q3ZMC M/B LA-8481P Schematic</b>	Rev 1.0
				Date: Thursday, April 12, 2012	Sheet 3 of 51

eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms, even if disable eDP function...

Add eDP circuit



<15> DMI\_CRX\_PTX\_N0  
<15> DMI\_CRX\_PTX\_N1  
<15> DMI\_CRX\_PTX\_N2  
<15> DMI\_CRX\_PTX\_N3  
  
<15> DMI\_CRX\_PTX\_P0  
<15> DMI\_CRX\_PTX\_P1  
<15> DMI\_CRX\_PTX\_P2  
<15> DMI\_CRX\_PTX\_P3  
  
<15> DMI\_CTX\_PRX\_N0  
<15> DMI\_CTX\_PRX\_N1  
<15> DMI\_CTX\_PRX\_N2  
<15> DMI\_CTX\_PRX\_N3  
  
<15> DMI\_CTX\_PRX\_P0  
<15> DMI\_CTX\_PRX\_P1  
<15> DMI\_CTX\_PRX\_P2  
<15> DMI\_CTX\_PRX\_P3

<15> FDI\_CTX\_PRX\_N0  
<15> FDI\_CTX\_PRX\_N1  
<15> FDI\_CTX\_PRX\_N2  
<15> FDI\_CTX\_PRX\_N3  
<15> FDI\_CTX\_PRX\_N4  
<15> FDI\_CTX\_PRX\_N5  
<15> FDI\_CTX\_PRX\_N6  
<15> FDI\_CTX\_PRX\_N7

<15> FDI\_CTX\_PRX\_P0  
<15> FDI\_CTX\_PRX\_P1  
<15> FDI\_CTX\_PRX\_P2  
<15> FDI\_CTX\_PRX\_P3  
<15> FDI\_CTX\_PRX\_P4  
<15> FDI\_CTX\_PRX\_P5  
<15> FDI\_CTX\_PRX\_P6  
<15> FDI\_CTX\_PRX\_P7

<15> FDI\_FSYNCO  
<15> FDI\_FSYNCO  
  
<15> FDI\_INT  
  
<15> FDI\_LSYNCO  
<15> FDI\_LSYNCO

<22> EDP\_AUXN  
<22> EDP\_AUXP  
  
<22> EDP\_TXN0  
<22> EDP\_TXN1  
  
<22> EDP\_TXP0  
<22> EDP\_TXP1

M2 DMI\_RX#0  
P6 DMI\_RX#1  
P10 DMI\_RX#2  
P10 DMI\_RX#3  
  
N3 DMI\_RX#0  
P7 DMI\_RX#1  
P3 DMI\_RX#2  
P11 DMI\_RX#3  
  
K1 DMI\_TX#0  
M6 DMI\_TX#1  
N4 DMI\_TX#2  
R2 DMI\_TX#3  
  
K3 DMI\_TX#0  
M7 DMI\_TX#1  
P4 DMI\_TX#2  
T3 DMI\_TX#3

U7 FDI0\_TX#0  
W11 FDI0\_TX#1  
AA6 FDI0\_TX#2  
W6 FDI0\_TX#3  
V4 FDI1\_TX#0  
Y2 FDI1\_TX#1  
AC9 FDI1\_TX#2  
AC9 FDI1\_TX#3

U6 FDI0\_TX#0  
W10 FDI0\_TX#1  
W3 FDI0\_TX#2  
AA7 FDI0\_TX#3  
W7 FDI1\_TX#0  
T4 FDI1\_TX#1  
AA3 FDI1\_TX#2  
AC8 FDI1\_TX#3

AA11 FDI0\_FSYNCO  
AC12 FDI1\_FSYNCO  
  
U11 FDI\_INT  
  
AA10 FDI0\_LSYNCO  
AG8 FDI1\_LSYNCO

AF3 eDP\_COMPIO  
AD2 eDP\_ICOMPO  
AG11 eDP\_HPDP#

AG4 eDP\_AUX#  
AF4 eDP\_AUX

AC3 eDP\_TX#0  
AC4 eDP\_TX#1  
AE11 eDP\_TX#2  
AE7 eDP\_TX#3

AC1 eDP\_TX#0  
AA4 eDP\_TX#1  
AE10 eDP\_TX#2  
AE6 eDP\_TX#3

IVY-BRIDGE\_BGA1023  
IVB@

ULV type P/N:

- 1.SA00005B000:S IC AV8063801057400 QBP7 K0 1.7G BGA  
2.SA00005AZ30:S IC AV8063801057401 QBTP K0 1.5G BGA

DMI

FDI (R) IAU1

FDI

PCI EXPRESS -- GRAPHICS

PEG\_ICOMPI  
PEG\_ICOMPO  
PEG\_RCOMPO

PEG\_RX#0  
PEG\_RX#1  
PEG\_RX#2  
PEG\_RX#3  
PEG\_RX#4  
PEG\_RX#5  
PEG\_RX#6  
PEG\_RX#7  
PEG\_RX#8  
PEG\_RX#9  
PEG\_RX#10  
PEG\_RX#11  
PEG\_RX#12  
PEG\_RX#13  
PEG\_RX#14  
PEG\_RX#15

PEG\_RX#0  
PEG\_RX#1  
PEG\_RX#2  
PEG\_RX#3  
PEG\_RX#4  
PEG\_RX#5  
PEG\_RX#6  
PEG\_RX#7  
PEG\_RX#8  
PEG\_RX#9  
PEG\_RX#10  
PEG\_RX#11  
PEG\_RX#12  
PEG\_RX#13  
PEG\_RX#14  
PEG\_RX#15

PEG\_TX#0  
PEG\_TX#1  
PEG\_TX#2  
PEG\_TX#3  
PEG\_TX#4  
PEG\_TX#5  
PEG\_TX#6  
PEG\_TX#7  
PEG\_TX#8  
PEG\_TX#9  
PEG\_TX#10  
PEG\_TX#11  
PEG\_TX#12  
PEG\_TX#13  
PEG\_TX#14  
PEG\_TX#15

PEG\_TX#0  
PEG\_TX#1  
PEG\_TX#2  
PEG\_TX#3  
PEG\_TX#4  
PEG\_TX#5  
PEG\_TX#6  
PEG\_TX#7  
PEG\_TX#8  
PEG\_TX#9  
PEG\_TX#10  
PEG\_TX#11  
PEG\_TX#12  
PEG\_TX#13  
PEG\_TX#14  
PEG\_TX#15

G3  
G1  
G4

PEG\_COMP

G3, W=4mil, S=15mil, L=500mil  
G1, W=12mil, S=15mil, L=500mil  
G4, W=4mil, S=15mil, L=500mil

UMA only=>PEG NC

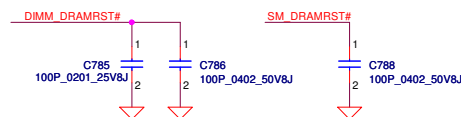
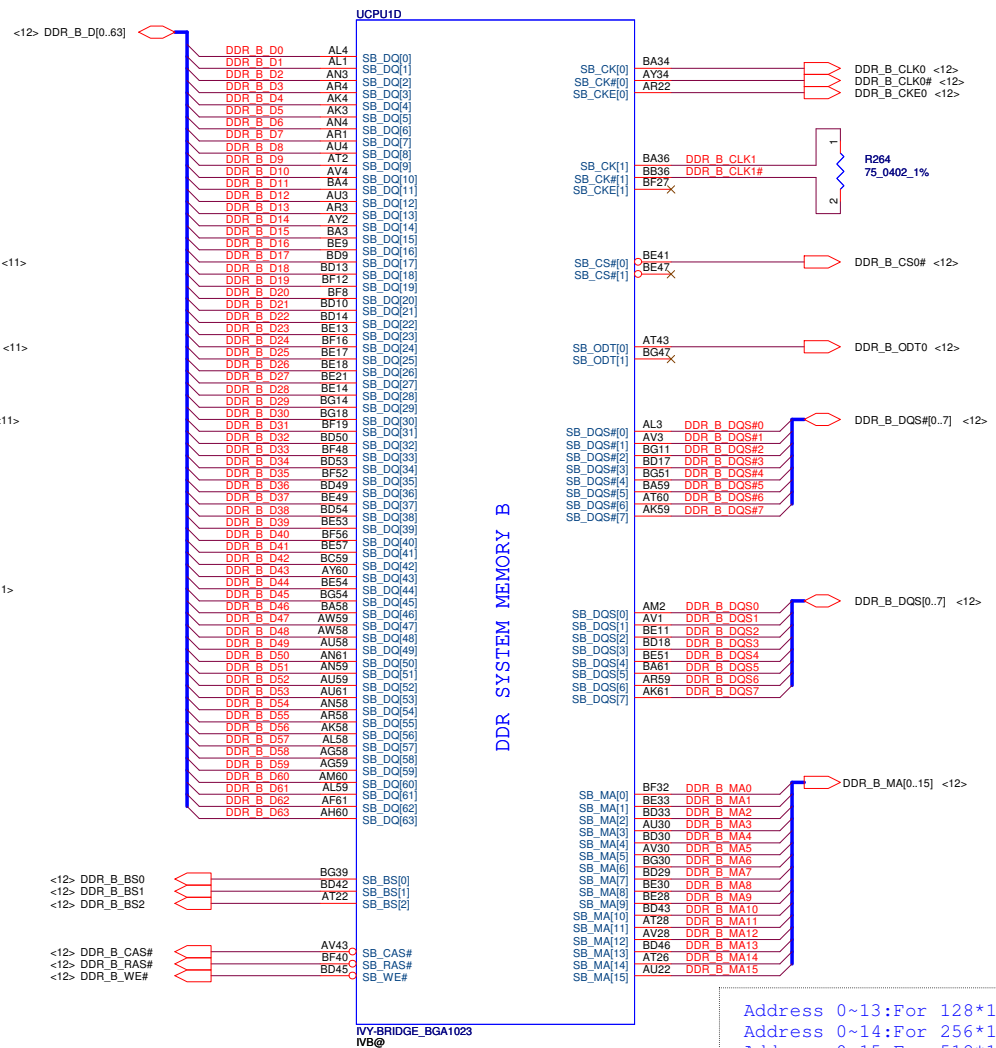
PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms

PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		2012/4/6	Deciphered Date	2013/4/6	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					PROCESSOR(1/7) DMI,FDI,PEG		
					Size	Document Number	Rev
					Custom	Q3ZMC M/B LA-8481P Schematic	1.0
					Date:	Thursday, April 12, 2012	Sheet 4 of 51

**Follow DG 1.2 & CRB1.0**

Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>PROCESSOR(2/7) PM,XDP,CLK</b>		
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF PRODUCT DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Docu	Document Number	Rev
				Custom	<b>Q3ZMC M/B LA-8481P Schematic</b>	1.0
				Date:	Thursday, April 12, 2012	Sheet 5 of 51

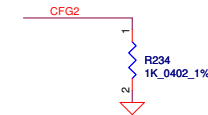


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	PROCESSOR(3/7) DDRIII	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Docu	Document Number	Rev
				Customer	Q32MC M/B LA-8481P Schematic	1.0
Date:	Tuesday, April 12, 2012	Sheet	6	of	51	

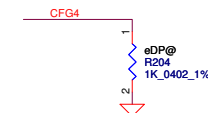
## CFG Straps for Processor

## PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed
------	--

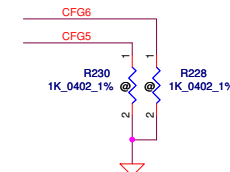


eDP enable	★ 1: Disable 0: Enable
------------	---------------------------



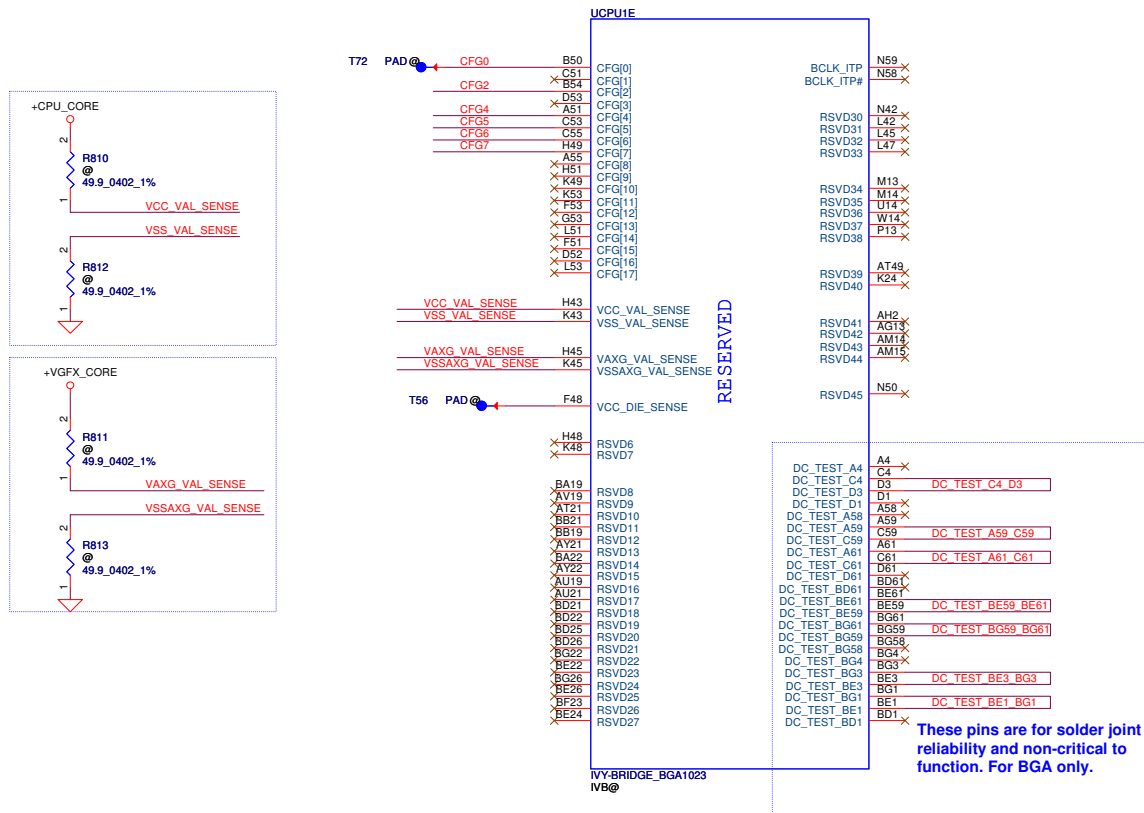
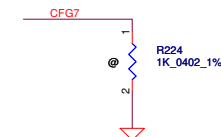
## PCIe Port Bifurcation Straps

CFG[6:5]	★ 11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express
----------	--

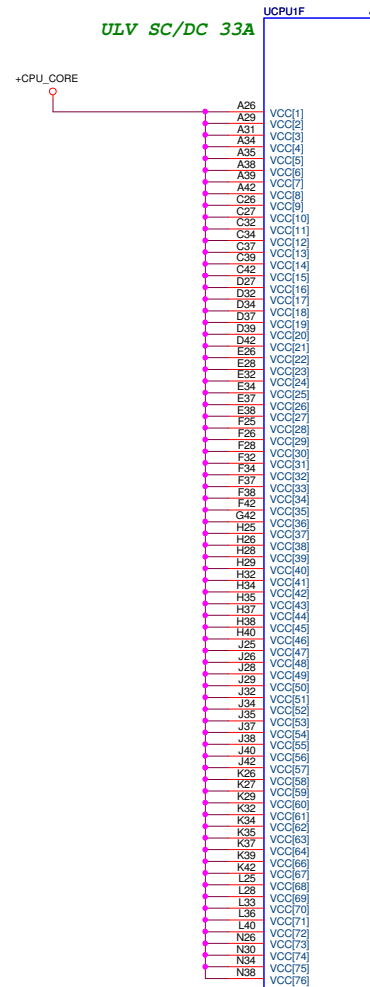


## PEG DEFER TRAINING CRB1.0 P.12

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	---



INTEL Recommend VCC  
3\*330uF,12\*22uF(0805),16\*2.2uF(0402)  
PD0.9



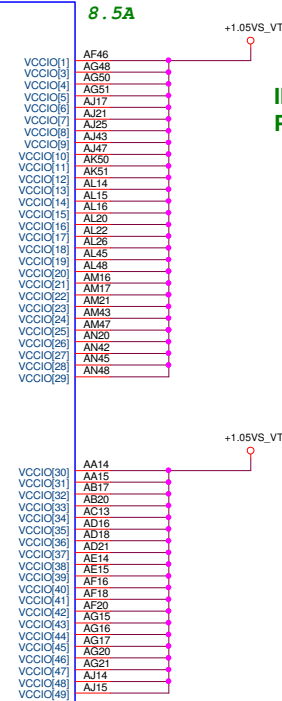
CORE SUPPLY

PEG IO AND DDR IO

QUIET RAILS

SVID

SENSE LINES



INTEL Recommend VCCIO  
PD 0.9

330uF 1+1  
10uF (0603) \*5  
1uF (0201) \*16

330uF 1  
10uF (0603) \*5  
1uF (0201) \*10

VCCIO_SEL For 2012 CPU support	
A19	* 1 : +1.05VS_VTT 0 : +1.0VS_VTT

Check List R1.5  
VIDALERT#: 75ohm  $\pm 5\%$  pull-up to VCCIO close to IMVP7  
VIDSCLK: 55ohm  $\pm 5\%$  pull-up to VCCIO close to IMVP7  
VIDSOUT: 130ohm  $\pm 5\%$  pull-up to VCCIO close to CPU  
130ohm  $\pm 5\%$  pull-up to VCCIO close to IMVP7

Check List R1.5  
VCCSENSE: 100ohm  $\pm 1\%$  pull-up to VCC near processor.  
VSSSENSE: 100ohm  $\pm 1\%$  pull-down to GND near processor.

Place the PU,PD resistors close to CPU

Should change to connect from power circuit & layout differential with VCCIO\_SENSE.

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/4/6	Deciphered Date	2013/4/6	PROCESSOR(5/7) PWR,BYPASS	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number Q32MC M/B LA-8481P Schematic
				Date: Thursday, April 12, 2012	Rev 1.0
				Sheet 8	of 51

INTEL Recommend VAXG  
2\*330uF,5\*22uF(0805),6\*10uF(0603),6\*1uF(0402)  
PD 0.9

Check List R1.5  
VCCAXG\_SENSE:100ohm  $\pm 5\%$  pull-up to VCC near processor.  
VSSAXG\_SENSE:100ohm  $\pm 5\%$  pull-down to GND near processor.

INTEL Recommend VCCPLL  
1\*330uF,2\*1uF(0402)  
PD 0.9

INTEL Recommend VCCSA  
1\*330uF,5\*10uF(0603) ,5\*1uF(0402)  
PD0.9

ULV SC/DC GT1: 18A  
GT2: 33A

## POWER

SA\_DIMM\_VREFDQ  
SB\_DIMM\_VREFDQ  
For Future CPU M3 support,  
Sandy bridge not support M3,  
Check list1.0 & CRB say can NC

+V\_SM\_VREF should  
have 20 mil trace width

INTEL Recommend VDDQ  
1\*330uF,8\*10uF(0603) ,10\*1uF(0402)  
PD0.9

Short for +1.35VS to +1.35V\_CPU\_VDDQ

GRAPHICS

DDR3 - 1.5V RAILS

QUIET RAILS

SENSE LINES

1.8V RAIL

SA RAIL

VCCSA VID lines

VCCSA\_VID0 Must PD

VCCSA\_VID1

VCCSA\_VID2

VCCSA\_VID3

VCCSA\_VID4

VCCSA\_VID5

VCCSA\_VID6

VCCSA\_VID7

VCCSA\_VID8

VCCSA\_VID9

VCCSA\_VID10

VCCSA\_VID11

VCCSA\_VID12

VCCSA\_VID13

VCCSA\_VID14

VCCSA\_VID15

VCCSA\_VID16

VCCSA\_VID17

VCCSA\_VID18

VCCSA\_VID19

VCCSA\_VID20

VCCSA\_VID21

VCCSA\_VID22

VCCSA\_VID23

VCCSA\_VID24

VCCSA\_VID25

VCCSA\_VID26

VCCSA\_VID27

VCCSA\_VID28

VCCSA\_VID29

VCCSA\_VID30

VCCSA\_VID31

VCCSA\_VID32

VCCSA\_VID33

VCCSA\_VID34

VCCSA\_VID35

VCCSA\_VID36

VCCSA\_VID37

VCCSA\_VID38

VCCSA\_VID39

VCCSA\_VID40

VCCSA\_VID41

VCCSA\_VID42

VCCSA\_VID43

VCCSA\_VID44

VCCSA\_VID45

VCCSA\_VID46

VCCSA\_VID47

VCCSA\_VID48

VCCSA\_VID49

VCCSA\_VID50

VCCSA\_VID51

VCCSA\_VID52

VCCSA\_VID53

VCCSA\_VID54

VCCSA\_VID55

VCCSA\_VID56

VCCSA\_VID57

VCCSA\_VID58

VCCSA\_VID59

VCCSA\_VID60

VCCSA\_VID61

VCCSA\_VID62

VCCSA\_VID63

VCCSA\_VID64

VCCSA\_VID65

VCCSA\_VID66

VCCSA\_VID67

VCCSA\_VID68

VCCSA\_VID69

VCCSA\_VID70

VCCSA\_VID71

VCCSA\_VID72

VCCSA\_VID73

VCCSA\_VID74

VCCSA\_VID75

VCCSA\_VID76

VCCSA\_VID77

VCCSA\_VID78

VCCSA\_VID79

VCCSA\_VID80

VCCSA\_VID81

VCCSA\_VID82

VCCSA\_VID83

VCCSA\_VID84

VCCSA\_VID85

VCCSA\_VID86

VCCSA\_VID87

VCCSA\_VID88

VCCSA\_VID89

VCCSA\_VID90

VCCSA\_VID91

VCCSA\_VID92

VCCSA\_VID93

VCCSA\_VID94

VCCSA\_VID95

VCCSA\_VID96

VCCSA\_VID97

VCCSA\_VID98

VCCSA\_VID99

VCCSA\_VID100

VCCSA\_VID101

VCCSA\_VID102

VCCSA\_VID103

VCCSA\_VID104

VCCSA\_VID105

VCCSA\_VID106

VCCSA\_VID107

VCCSA\_VID108

VCCSA\_VID109

VCCSA\_VID110

VCCSA\_VID111

VCCSA\_VID112

VCCSA\_VID113

VCCSA\_VID114

VCCSA\_VID115

VCCSA\_VID116

VCCSA\_VID117

VCCSA\_VID118

VCCSA\_VID119

VCCSA\_VID120

VCCSA\_VID121

VCCSA\_VID122

VCCSA\_VID123

VCCSA\_VID124

VCCSA\_VID125

VCCSA\_VID126

VCCSA\_VID127

VCCSA\_VID128

VCCSA\_VID129

VCCSA\_VID130

VCCSA\_VID131

VCCSA\_VID132

VCCSA\_VID133

VCCSA\_VID134

VCCSA\_VID135

VCCSA\_VID136

VCCSA\_VID137

VCCSA\_VID138

VCCSA\_VID139

VCCSA\_VID140

VCCSA\_VID141

VCCSA\_VID142

VCCSA\_VID143

VCCSA\_VID144

VCCSA\_VID145

VCCSA\_VID146

VCCSA\_VID147

VCCSA\_VID148

VCCSA\_VID149

VCCSA\_VID150

VCCSA\_VID151

VCCSA\_VID152

VCCSA\_VID153

VCCSA\_VID154

VCCSA\_VID155

VCCSA\_VID156

VCCSA\_VID157

VCCSA\_VID158

VCCSA\_VID159

VCCSA\_VID160

VCCSA\_VID161

VCCSA\_VID162

VCCSA\_VID163

VCCSA\_VID164

VCCSA\_VID165

VCCSA\_VID166

VCCSA\_VID167

VCCSA\_VID168

VCCSA\_VID169

VCCSA\_VID170

VCCSA\_VID171

VCCSA\_VID172

VCCSA\_VID173

VCCSA\_VID174

VCCSA\_VID175

VCCSA\_VID176

VCCSA\_VID177

VCCSA\_VID178

VCCSA\_VID179

VCCSA\_VID180

VCCSA\_VID181

VCCSA\_VID182

VCCSA\_VID183

VCCSA\_VID184

VCCSA\_VID185

VCCSA\_VID186

VCCSA\_VID187

VCCSA\_VID188

VCCSA\_VID189

VCCSA\_VID190

VCCSA\_VID191

VCCSA\_VID192

VCCSA\_VID193

VCCSA\_VID194

VCCSA\_VID195

VCCSA\_VID196

VCCSA\_VID197

VCCSA\_VID198

VCCSA\_VID199

VCCSA\_VID200

VCCSA\_VID201

VCCSA\_VID202

VCCSA\_VID203

VCCSA\_VID204

VCCSA\_VID205

VCCSA\_VID206

VCCSA\_VID207

VCCSA\_VID208

VCCSA\_VID209

VCCSA\_VID210

VCCSA\_VID211

VCCSA\_VID212

VCCSA\_VID213

VCCSA\_VID214

VCCSA\_VID215

VCCSA\_VID216

VCCSA\_VID217

VCCSA\_VID218

VCCSA\_VID219

VCCSA\_VID220

VCCSA\_VID221

VCCSA\_VID222

VCCSA\_VID223

VCCSA\_VID224

VCCSA\_VID225

VCCSA\_VID226

VCCSA\_VID227

VCCSA\_VID228

VCCSA\_VID229

VCCSA\_VID230

VCCSA\_VID231

VCCSA\_VID232

VCCSA\_VID233

VCCSA\_VID234

VCCSA\_VID235

VCCSA\_VID236

VCCSA\_VID237

VCCSA\_VID238

VCCSA\_VID239

VCCSA\_VID240

VCCSA\_VID241

VCCSA\_VID242

VCCSA\_VID243

VCCSA\_VID244

VCCSA\_VID245

VCCSA\_VID246

VCCSA\_VID247

VCCSA\_VID248

VCCSA\_VID249

VCCSA\_VID250

VCCSA\_VID251

VCCSA\_VID252

VCCSA\_VID253

VCCSA\_VID254

VCCSA\_VID255

VCCSA\_VID256

VCCSA\_VID257

VCCSA\_VID258

VCCSA\_VID259

VCCSA\_VID260

VCCSA\_VID261

VCCSA\_VID262

VCCSA\_VID263

VCCSA\_VID264

VCCSA\_VID265

VCCSA\_VID266

VCCSA\_VID267

VCCSA\_VID268

VCCSA\_VID269

VCCSA\_VID270

VCCSA\_VID271

VCCSA\_VID272

VCCSA\_VID273

VCCSA\_VID274

VCCSA\_VID275

VCCSA\_VID276

VCCSA\_VID277

VCCSA\_VID278

VCCSA\_VID279

VCCSA\_VID280

VCCSA\_VID281

VCCSA\_VID282

VCCSA\_VID283

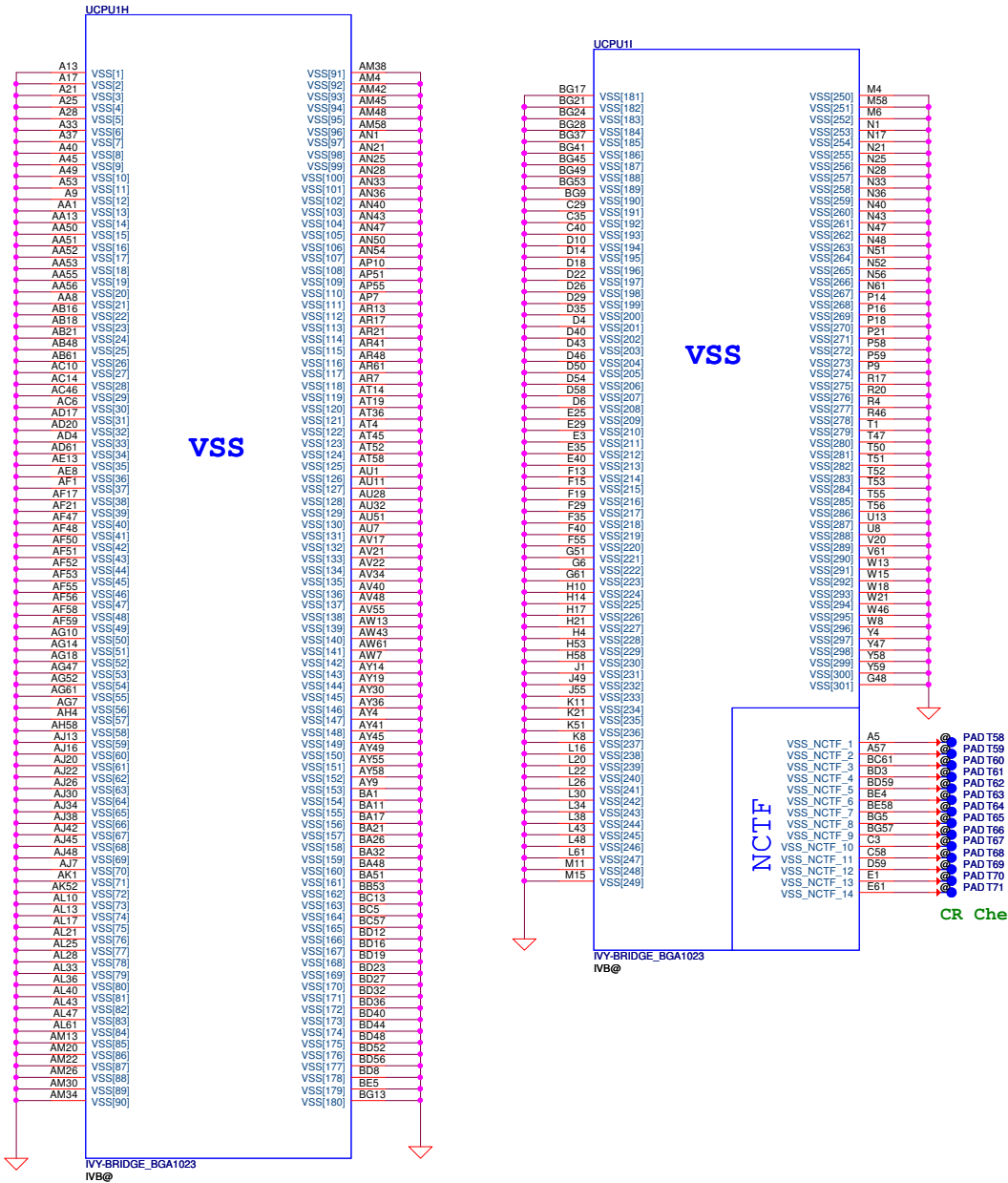
VCCSA\_VID284

VCCSA\_VID285

VCCSA\_VID286

VCCSA\_VID287

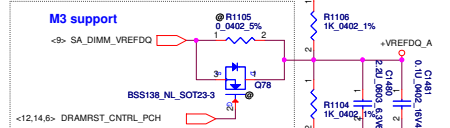
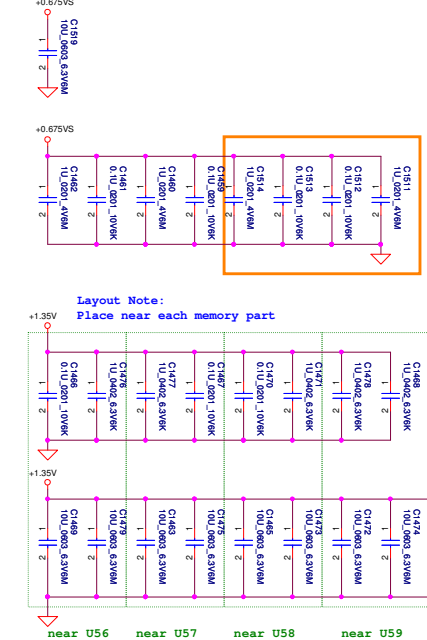
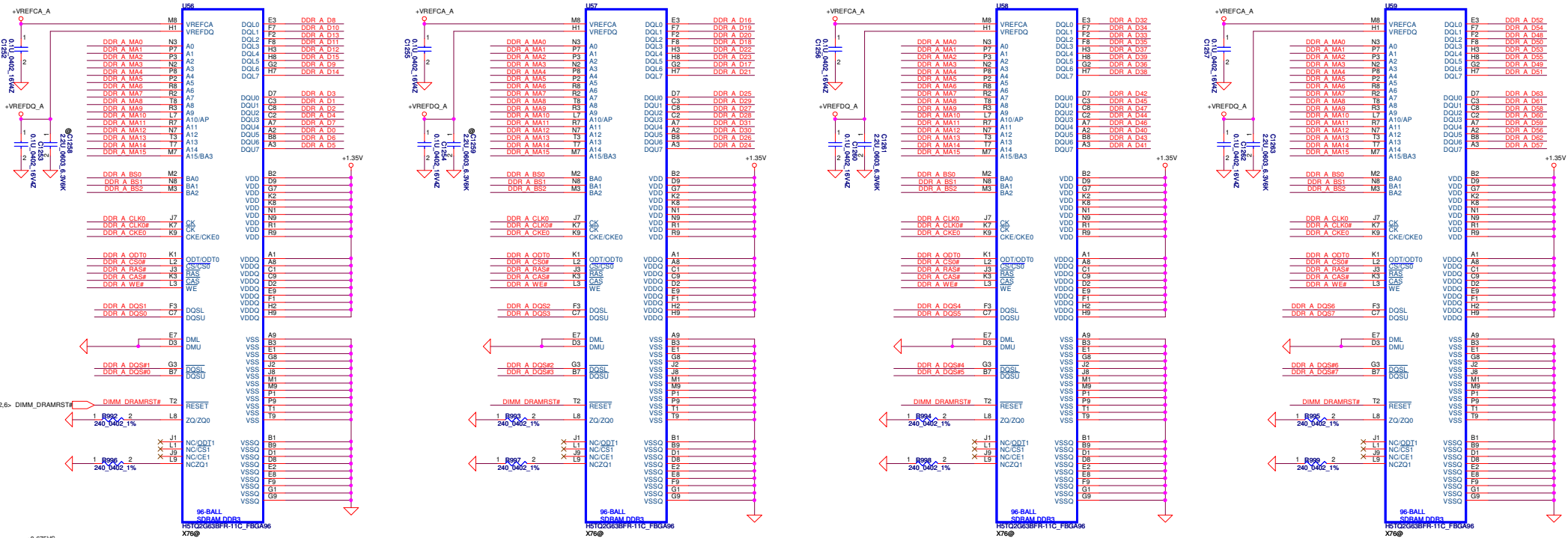
V



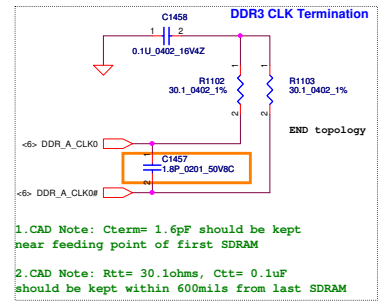
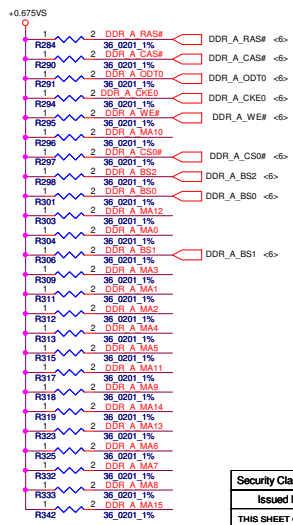
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2012/4/6		Title	
		Deciphered Date		PROCESSOR(7/7) VSS	
		2013/4/6		Document Number	
				Q3ZMC M/B LA-8481P Schematic	
				Rev	
				1.0	
				Date: Thursday, April 12, 2012	
				Sheet 10 of 51	

Channel A

<6> DDR\_A\_MA0[.15]

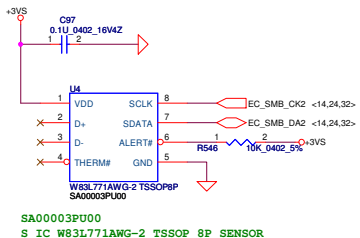


DDR3 CTL/ADD Termination

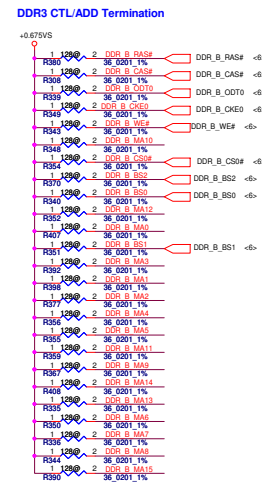
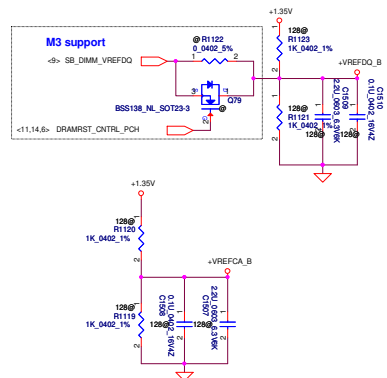
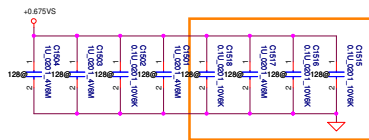


Delete U70 SPD EEROM circuit  
SA00004KS00  
S IC EE 2K AT24C02C-XHM-T TSSOP 8P

External DDR Thermal Sensor



DDR\_B\_DQS#[0..7] <6>  
DDR\_B\_DQS[0..7] <6>  
DDR\_B\_D[0..63] <6>  
DDR\_B\_MA[0..15] <6>

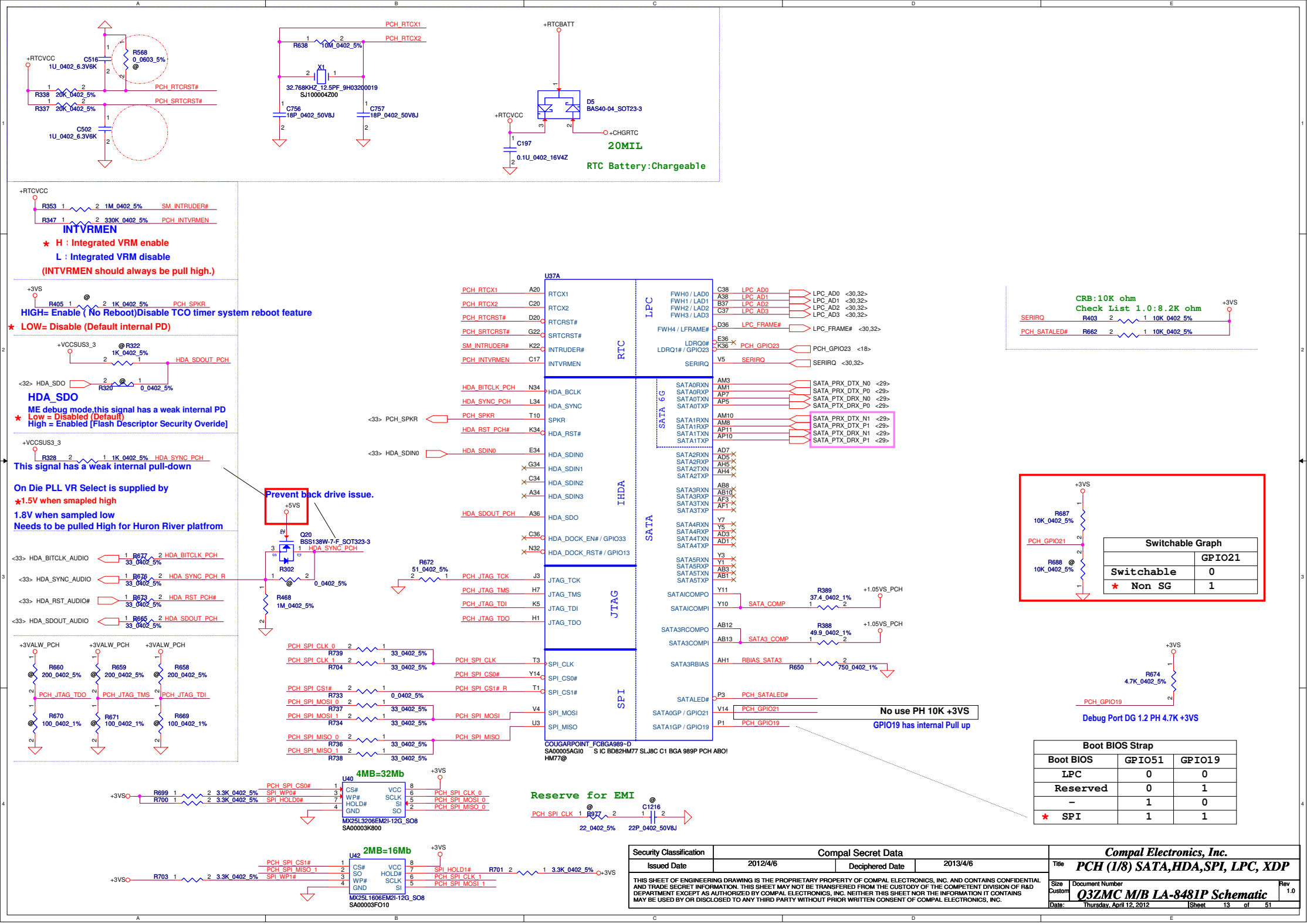


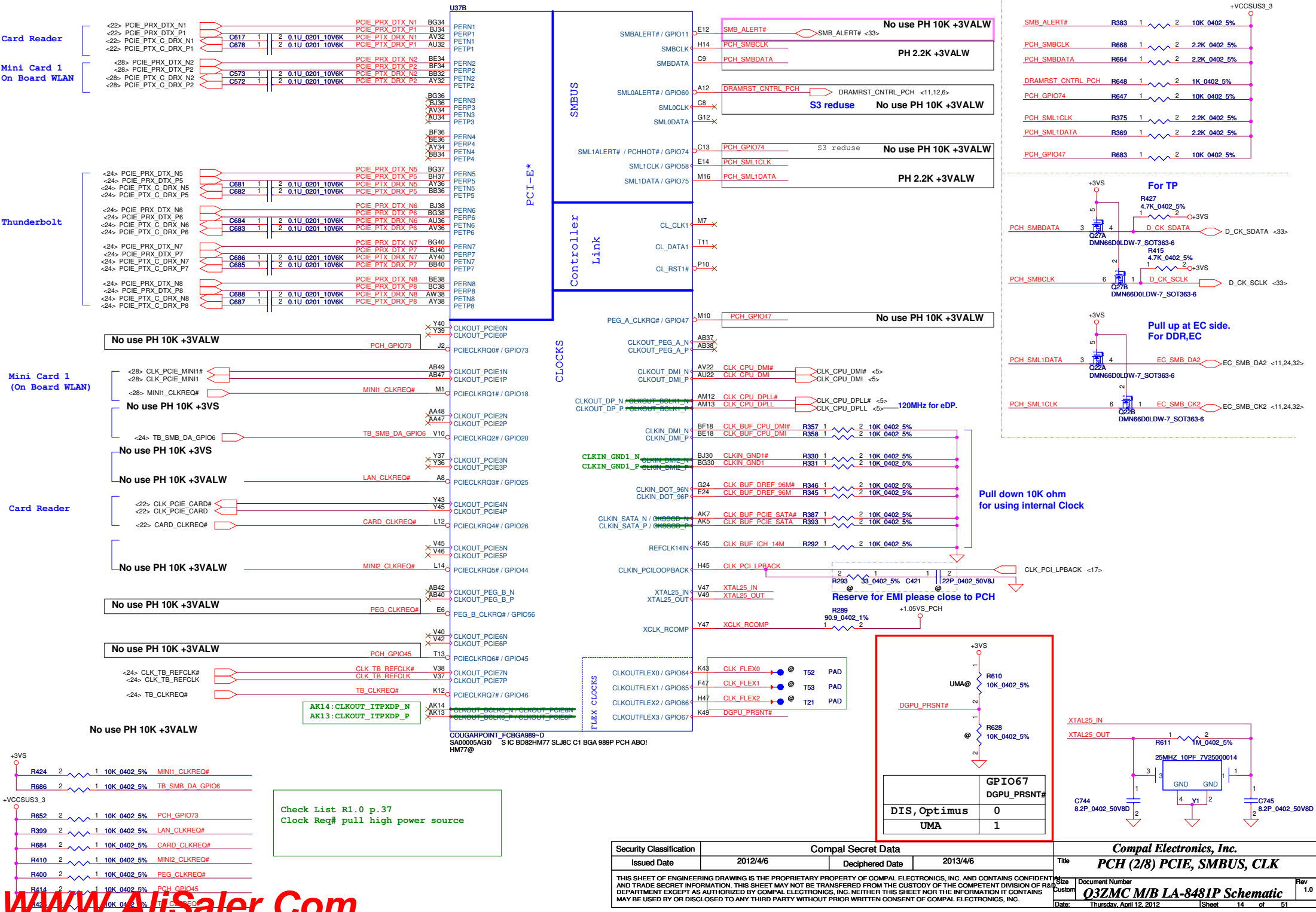
The diagram illustrates two methods for terminating the DDR3 clock signal (DDR3\_CLK0) at the SDRAM end. The top method uses a pi-network with two 128Ω resistors (R116, R117) in series with the signal line and a 0.1μF capacitor (C1506) connected to ground. The bottom method uses a single 128Ω resistor (R118) connected to ground. Both methods are labeled 'END topology'.

1. CAD Note: Cterm = 1.6pF should be kept near feeding point of first SDRAM

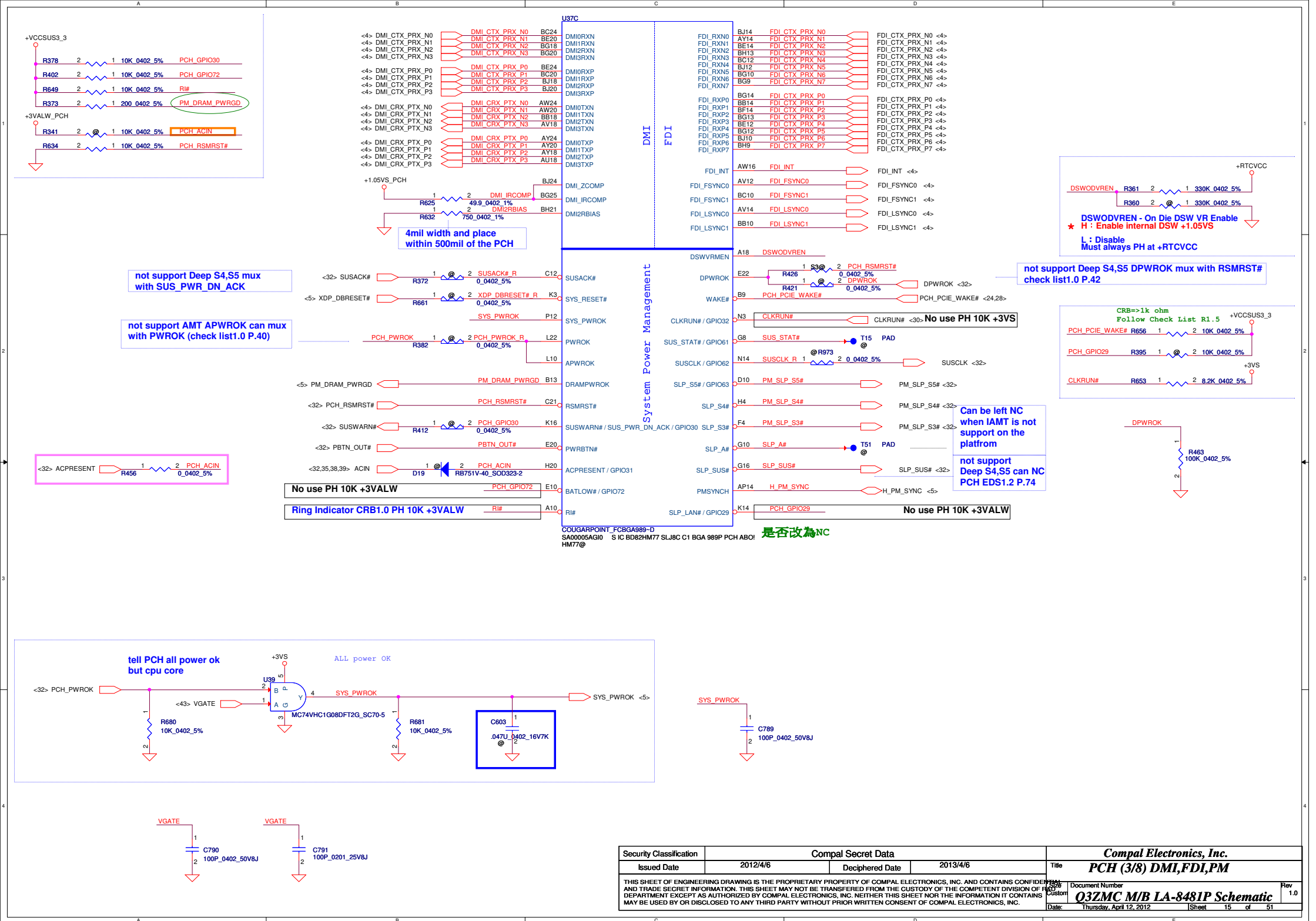
2. CAD Note: Rtt = 30.1ohms, Ctt = 0.1uF should be kept within 600mils from last SDRAM

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/4/6	Deciphered Date	2013/4/6	File
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D TO ANY OTHER DIVISION OR AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THE SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			DDRIII DIMMB	
			Docuement Number	
			Q3ZMC M/P LA-8481P Schematic Date: 2012/02/19	





Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2012/4/6		Deciphered Date		2013/4/6		Title		PCH (2/8) PCIE, SMBUS, CLK	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.											
Size		Document Number		Rev							
Custom		Q3ZMC M/B LA-8481P Schematic		1.0							
Date:		Thursday, April 12, 2012		Sheet		14		of		51	



# UMA Panel Backlight ON/OFF

<32> ENBKL ENBKL R612 2 @ 1 0\_0402\_5% IGPU BKLT\_EN

PD 100K  
at EC side

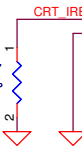
Delete LVDS function

LVDS disable:  
DATA/Clock/Control can NC  
VCC\_TX\_LVDS,VCCA\_LVDS connected to GND

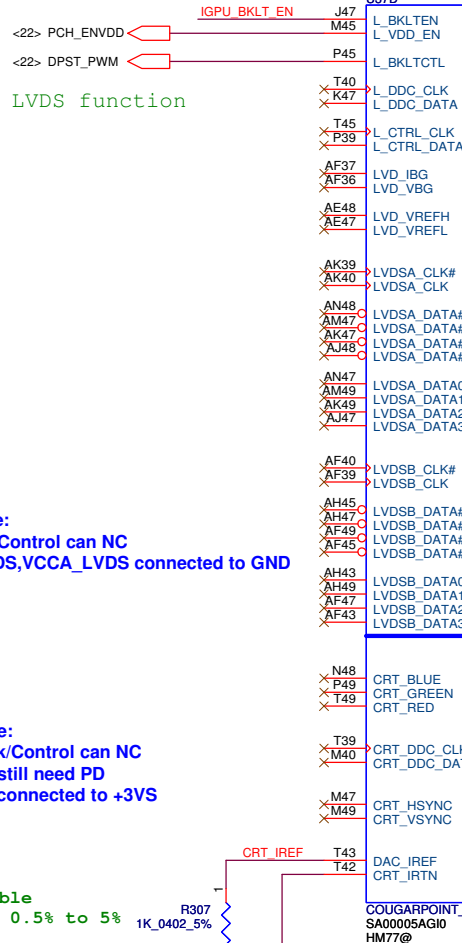
CRT disable:  
DATA/Clock/Control can NC  
DAC\_IREF still need PD  
VCCADAC connected to +3VS

For CRT diable  
=>Change 1K 0.5% to 5%

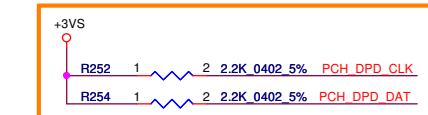
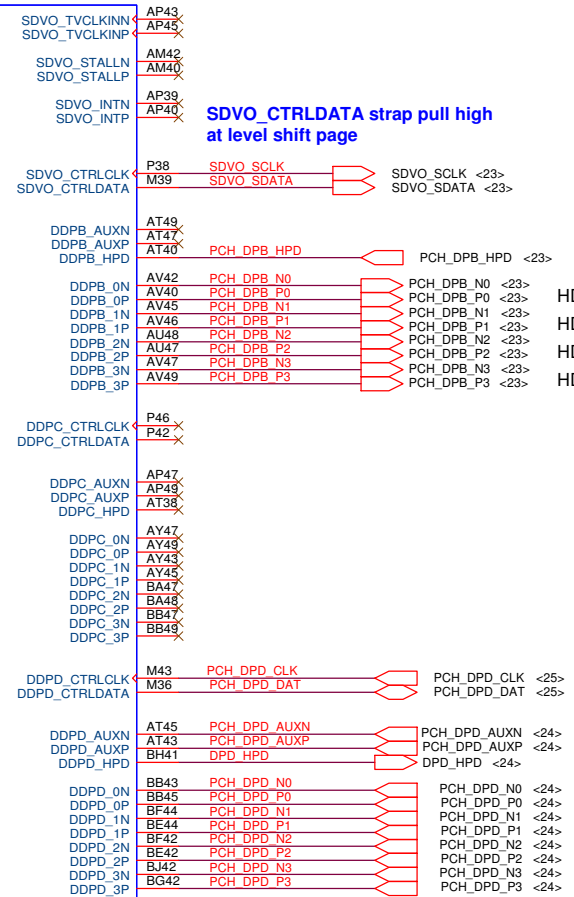
R307 1K\_0402\_5%



U37D



Digital Display Interface



Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2012/4/6		Deciphered Date		2013/4/6		Title			
								PCH (4/9) LVDS,CRT,DP,HDMI			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						Size	Document Number	Rev			
						Custom	Q3ZMC M/B LA-8481P Schematic	1.0			
						Date:	Thursday, April 12, 2012	Sheet	16	of	51

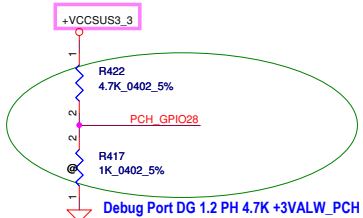


# HDA\_SYNC PH(PLL =+1.5VS)

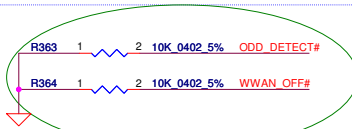
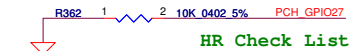
## GPIO28

### On-Die PLL Voltage Regulator

This signal has a weak internal pull up  
 \* H : On-Die PLL voltage regulator enable  
 L : On-Die PLL Voltage Regulator disable



Deep S4,S5 wake event signal  
 RTC alarm,Power BTN,GPIO27  
 PCH\_GPIO27 (Have internal Pull-High)  
 Deep S4,S5 wake event signal  
 No use PD to GND,HR Check list1.0 P.70

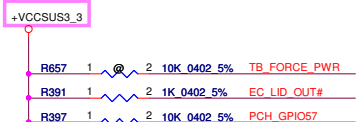
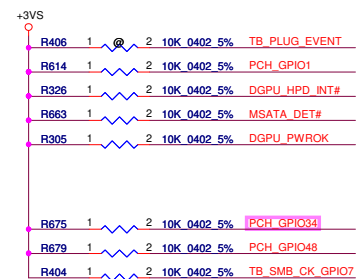


## SATA2GP/GPIO36,SATA3GP/GPIO37

1.Used as for Mechanical Presence detect -  
 Use a weak external pull-up (150K-200K Ohms) to Vcc3\_3  
 or use 10K external pull-up that is enabled only  
 after PLTRST# de-assertion.

2.Used as GP Input (Pin HW default) -  
 Ensure GPI is not driven high during strap sampling window

3.Unused as GPIO or SATA\*GP -  
 Use 8.2K-10K pull-down to ground.



GPIO24 Unmultiplexed  
 NOTE: GPIO24 configuration  
 register bits are not cleared by  
 CF9h reset event.  
 CRB1.0 PH10K to +3VALW

No use PH 10K +3VS	<24> TB_PLUG_EVENT	TB_PLUG_EVENT	T7
No use PH 10K +3VS	PCH_GPIO1	PCH_GPIO1	A42
No use PH 10K +3VS	DGPU_HPD_INT#	DGPU_HPD_INT#	H36

No use PH +3VALW	<24> TB_FORCE_PWR	TB_FORCE_PWR	C4
No use PH +3VALW	EC LID SW OUT	EC_LID_OUT#	G2
No use PH +3VS	<29> MSATA_DET#	MSATA_DET#	U2

No use PH 10K +3VS	PCH_GPIO22	PCH_GPIO22	T5
CRB1.0 PH 10K +3VALW	PCH_GPIO24	PCH_GPIO24	E8
No use PD 10K to GND	PCH_GPIO27	PCH_GPIO27	E16
No use PH 10K +3VALW	PCH_GPIO28	PCH_GPIO28	P8
No use PH 10K +3VS	PCH_GPIO34	PCH_GPIO34	K1
No use can NC(+3VS power plane)	RAID0_DET	RAID0_DET	K4
Can't PH	ODD_DETECT#	ODD_DETECT#	V8
Can't PH	WWAN_OFF#	WWAN_OFF#	M5
No use PH 10K +3VS Optimus(L)/ non optimus(H)	OPTIMUS_EN#	OPTIMUS_EN#	N2
No use PH 10K +3VS	PCH_GPIO39	PCH_GPIO39	M3
No use PH 10K +3VS	PCH_GPIO48	PCH_GPIO48	V13
SATA5GP&TEMP_ALERT# CRB PH 10K +3VS	TB_SMB_CK_GPIO7	TB_SMB_CK_GPIO7	V3
No use PH +3VALW	PCH_GPIO57	PCH_GPIO57	D6

GPIO38	OPTIMUS_EN#
Muxless	0
nonMuxless	1

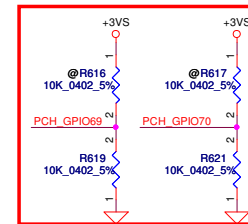
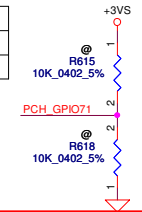
## Define Q5LJ1 (DDR3) or Q3ZMC (DDR3L)

GPIO24	PCH_GPIO24
DDR3L(Q3ZMC)	0
DDR3	1

GPIO36/GPIO37 is Strap functionality  
 that requires internal pull down to be sampled at rising PWROK.  
 When uses as SATA2GP/SATA3GP for mechanical presence detect  
 -use a external pull up 150K-200K ohm to Vcc3\_3  
 When used as GP input  
 -ensure GPI is not driven high during strap sampling window  
 When Unused as GPIO or SATA\*GP  
 -use 8.2K-10K pull-down  
 check list page 47

LVDS/eDP	GPIO71
LVDS	1
eDP	0

For eDP only,  
 不判断eDP or LVDS



Project ID	GPIO69	GPIO70
* x	0	0
x	0	1
x	1	0
x	1	1

## U37F

BMBUSY# / GPIO0	TACH4 / GPIO68
TACH1 / GPIO1	TACH5 / GPIO69
TACH2 / GPIO6	TACH6 / GPIO70
TACH3 / GPIO7	TACH7 / GPIO71
GPIO8	
LAN_PHY_PWR_CTRL / GPIO12	
GPIO15	
SATA4GP / GPIO16	
TACH0 / GPIO17	
SCLOCK / GPIO22	
GPIO24 / MEM_LED	
GPIO27	
GPIO28	
STP_PC# / GPIO34	
GPIO35	
SATA2GP / GPIO36	
SATA3GP / GPIO37	
SLOAD / GPIO38	
SDATAOUT0 / GPIO39	
SDATAOUT1 / GPIO48	
SATA5GP / GPIO49	
GPIO57	

## GPIO

## NCTF

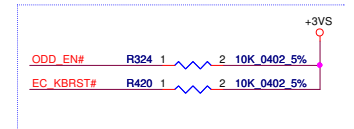
VSS_NCTF_1	BG2
VSS_NCTF_2	BG48
VSS_NCTF_3	BH3
VSS_NCTF_4	BH47
VSS_NCTF_5	BJ4
VSS_NCTF_6	BJ44
VSS_NCTF_7	BJ45
VSS_NCTF_8	BJ46
VSS_NCTF_9	BJ5
VSS_NCTF_10	BJ6
VSS_NCTF_11	C2
VSS_NCTF_12	C48
VSS_NCTF_13	D1
VSS_NCTF_14	D49
	E1
	E49
	F1
	F49

COUGARPOINT\_FCBGA888-D  
 SA00005AGIO S IC BD82HM77 SLJ8C C1 BGA 989P PCH ABOI  
 HM77@

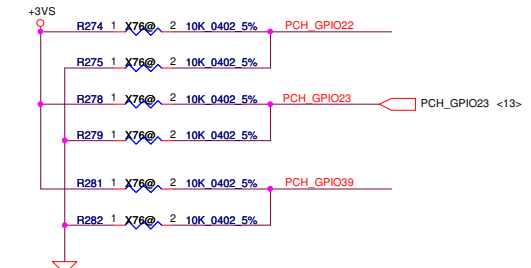
Remove NCTF test point  
 2011/9/23

INIT3\_3V Check list1.0 P.59  
 This signal has weak internal  
 PU, can't pull low,leave NC

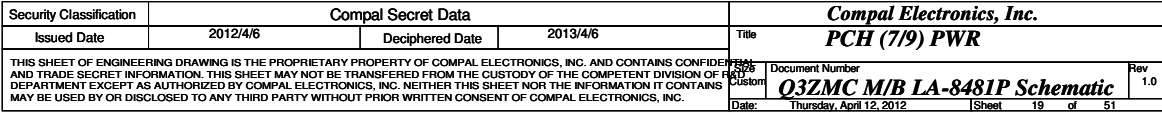
TS\_VSS1~4  
 PD to GND

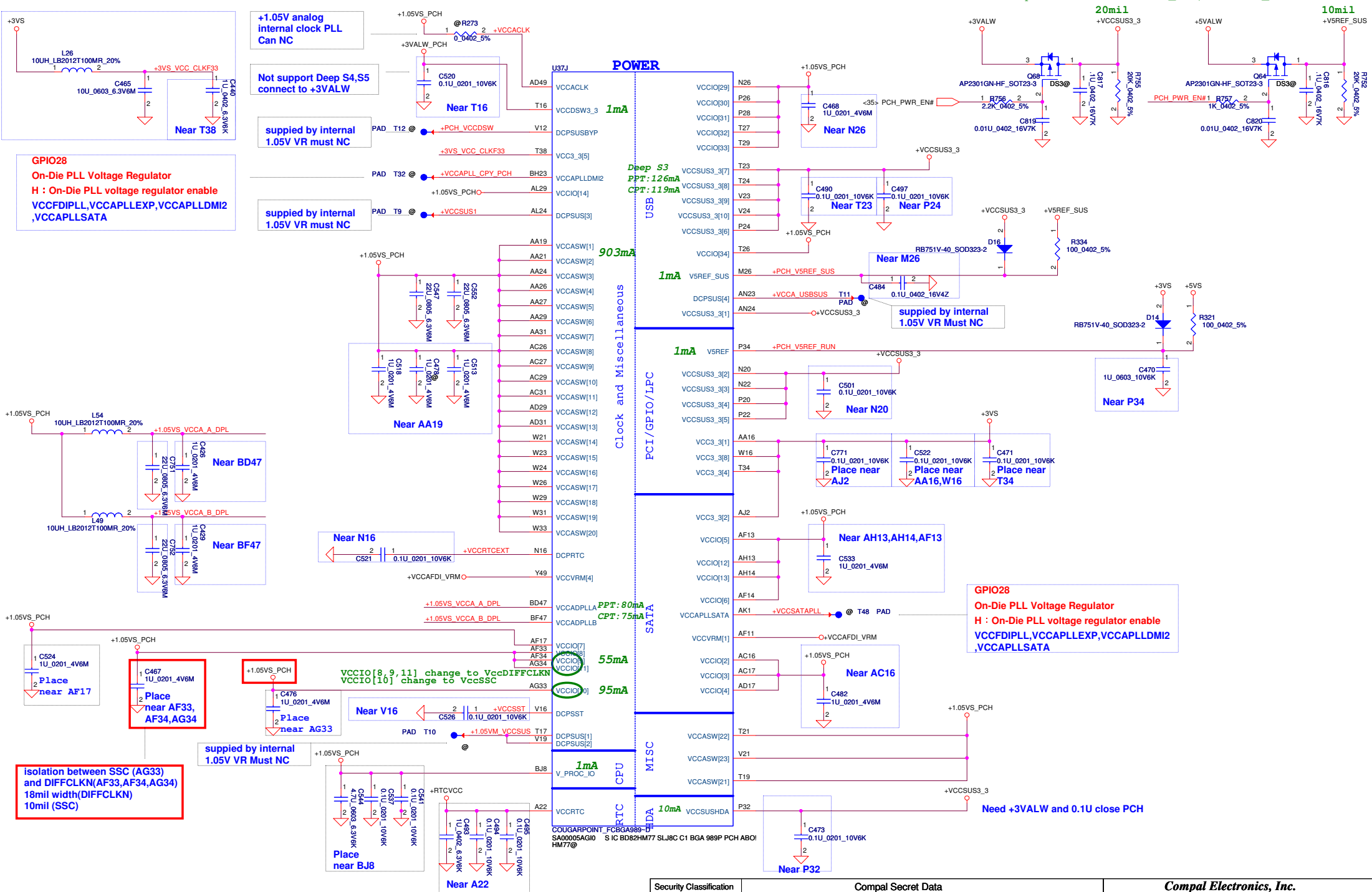


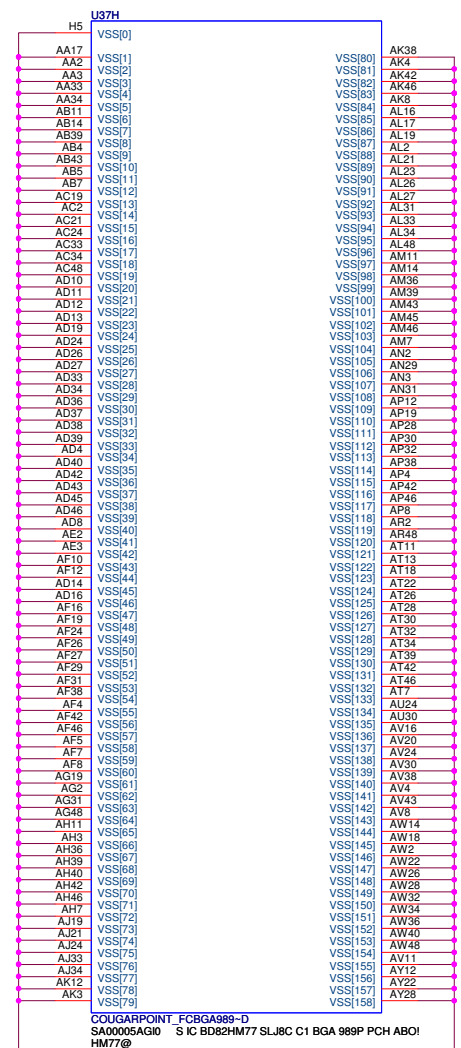
	GPIO39	GPIO23	GPIO22
Elpida DDP 1GB*8 (Ch A,B)	0	0	0
Elpida DDP 1GB*4 (Ch A)	0	0	1
Elpida Mono 512MB*8 (Ch A,B)	0	1	0
Hynix Mono 512MB*8 (Ch A,B)	0	1	1



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/4/6	Deciphered Date	2013/4/6	PCH (6/9) GPIO, CPU, MISC		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Revision	Rev
				Q3ZMC M/B LA-8481P Schematic	1.0	1.0
				Date: Thursday, April 12, 2012	Sheet	18 of 51





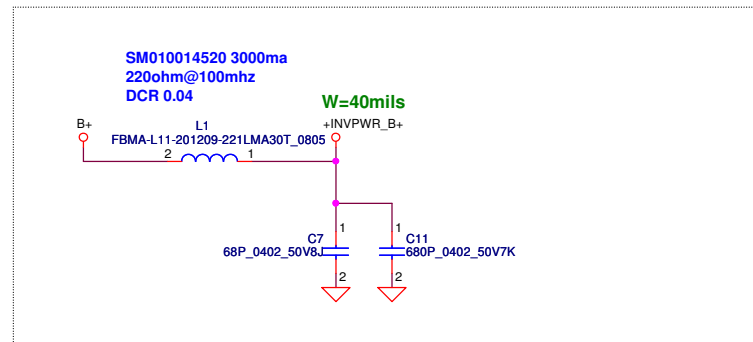
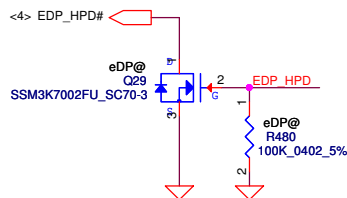
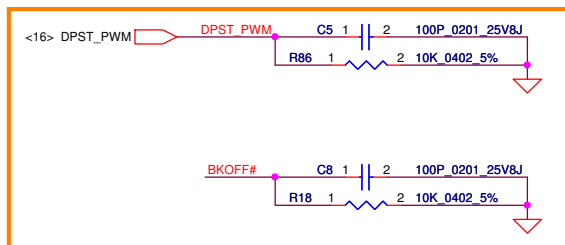
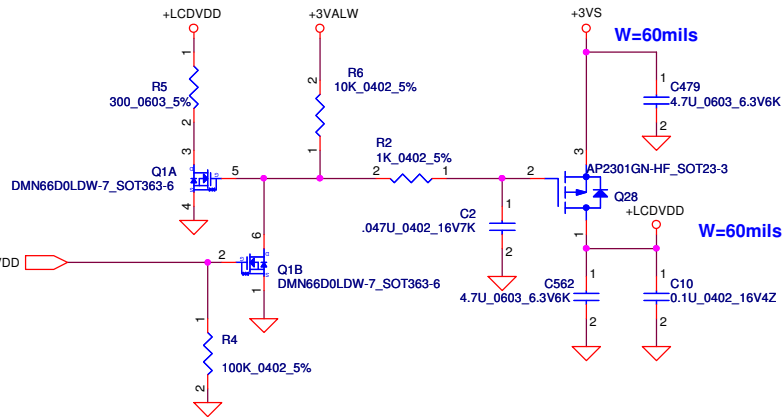


COUGARPOINT\_FCBGA989-D  
SA00005AG10 S IC BD82HM77 SLJ8C C1 BGA 989P PCH ABO!  
HM77@

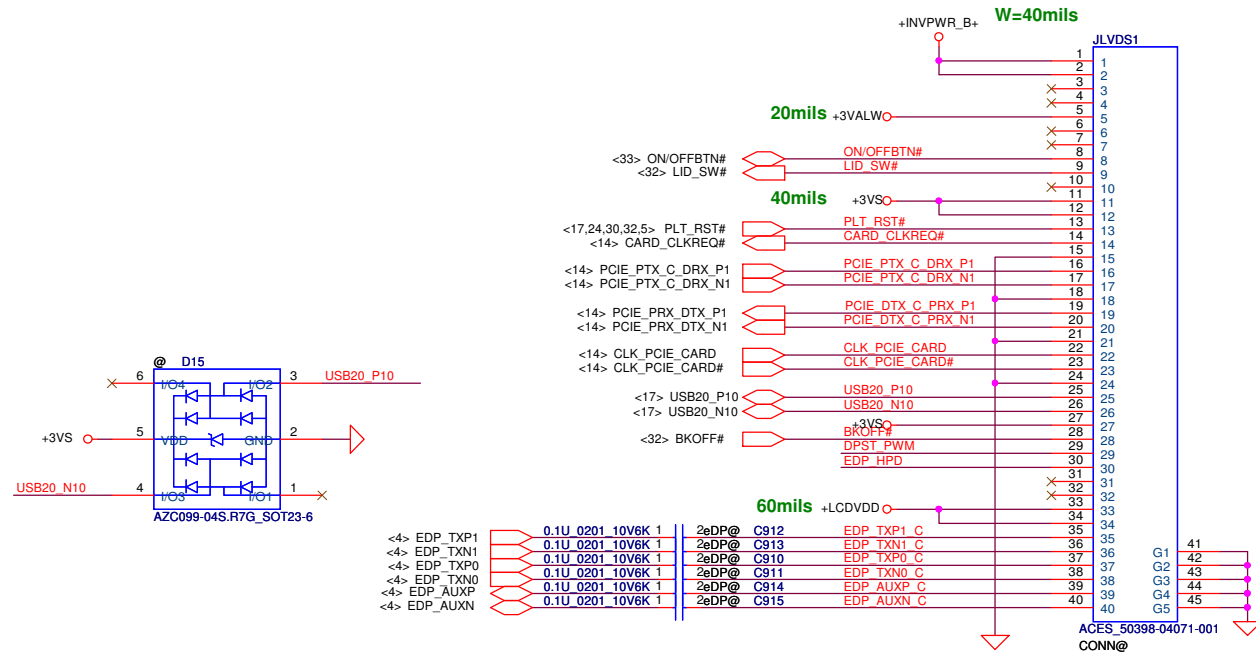
COUGARPOINT\_FCBGA989-D  
SA00005AG10 S IC BD82HM77 SLJ8C C1 BGA 989P PCH ABO!  
HM77@

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2012/4/6		Deciphered Date		2013/4/6		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Revision		Document Number		Rev		1.0	
				Date:		Thursday, April 12, 2012		Sheet		21 of 51	

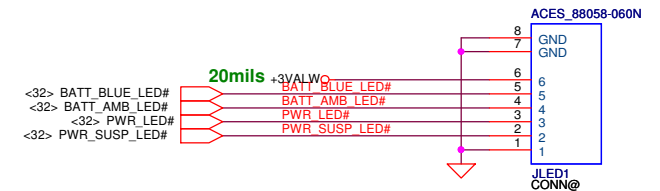
## Panel POWER CIRCUIT



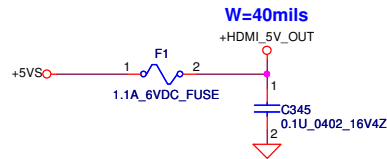
## eDP panel + Card Reader Conn.



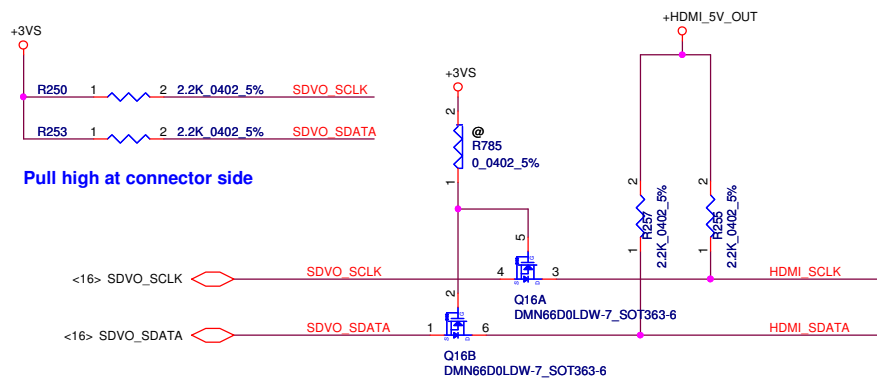
## To LED/B Conn.



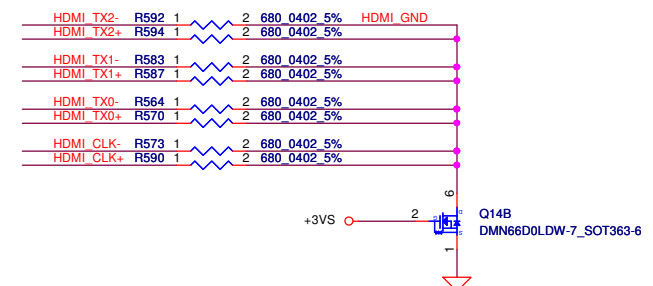
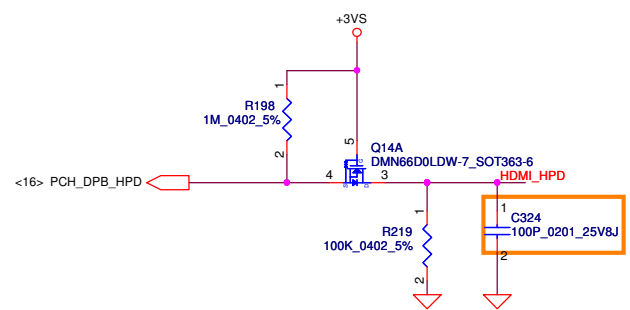
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	LVDS Connector
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Rev 1.0
Size	Document Number	Customer	Q3ZMC M/B LA-8481P Schematic	Date	Thursday, April 12, 2012
Sheet	22	of	51	Sheet	22 of 51



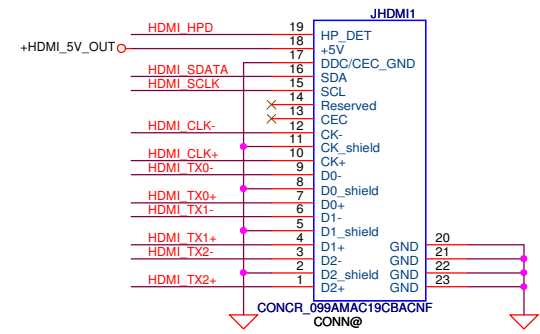
<16> PCH_DPB_N0	C280	2	1	.1U_0402_16V7K	HDMI TX2-
<16> PCH_DPB_P0	C281	2	1	.1U_0402_16V7K	HDMI TX2+
<16> PCH_DPB_N1	C283	2	1	.1U_0402_16V7K	HDMI TX1-
<16> PCH_DPB_P1	C282	2	1	.1U_0402_16V7K	HDMI TX1+
<16> PCH_DPB_N2	C287	2	1	.1U_0402_16V7K	HDMI TX0-
<16> PCH_DPB_P2	C286	2	1	.1U_0402_16V7K	HDMI TX0+
<16> PCH_DPB_N3	C285	2	1	.1U_0402_16V7K	HDMI CLK-
<16> PCH_DPB_P3	C284	2	1	.1U_0402_16V7K	HDMI CLK+



Place close to JHDMI1



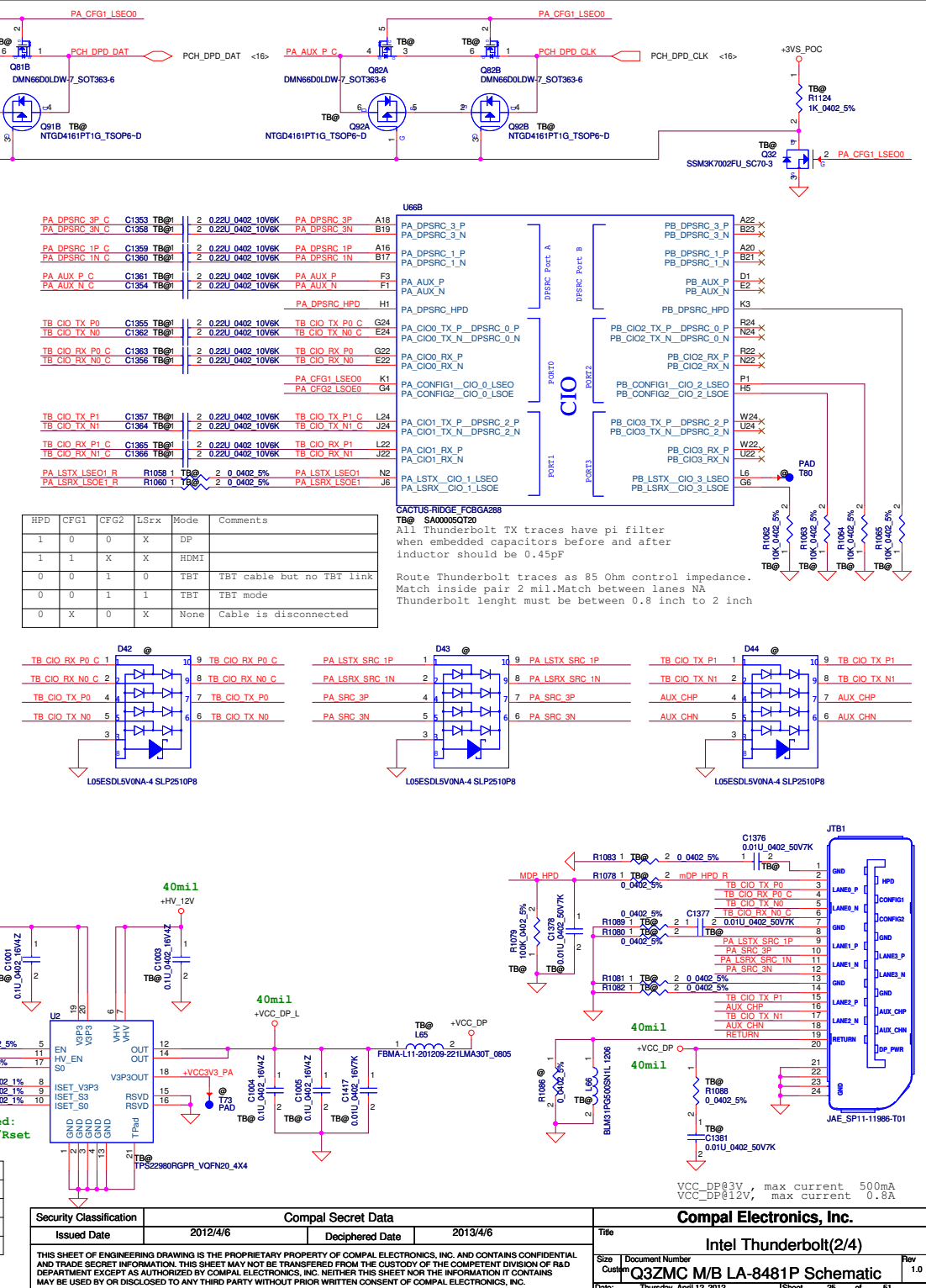
### HDMI connector



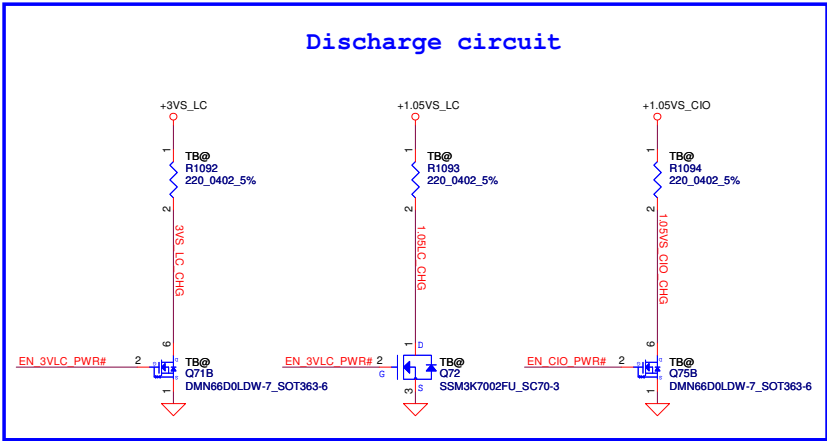
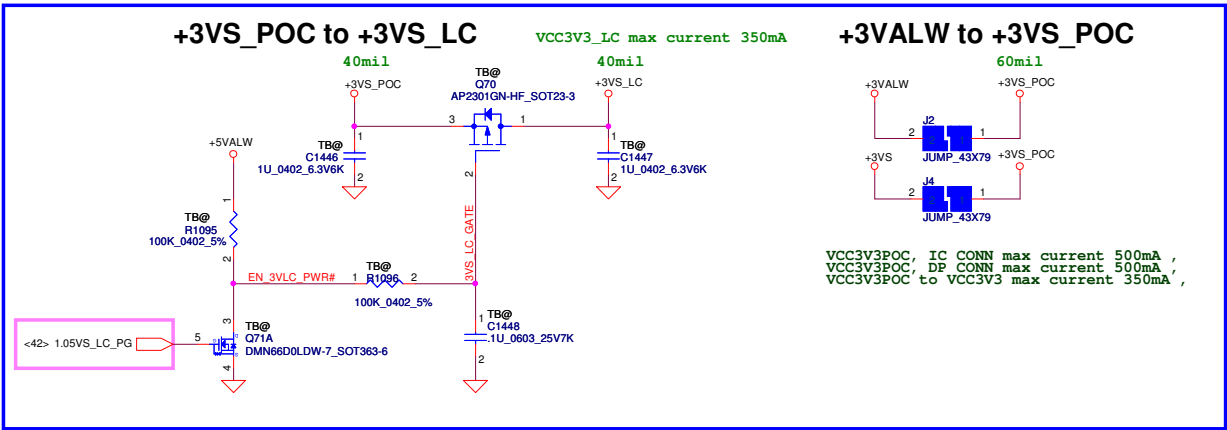
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	HDMI Connector	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	Q3ZMC M/B LA-8481P Schematic	1.0
				Date:	Thursday, April 12, 2012	Sheet 23 of 51



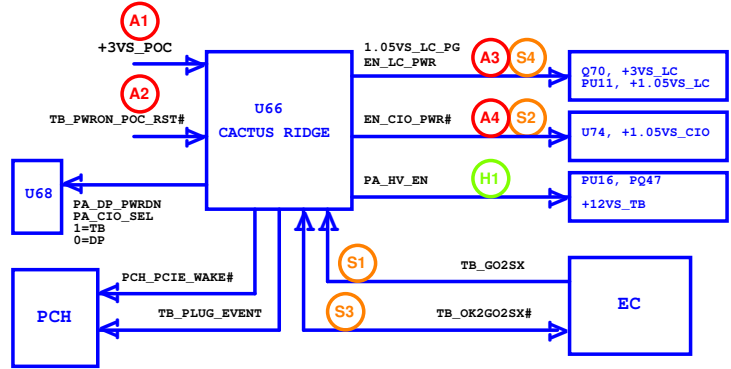
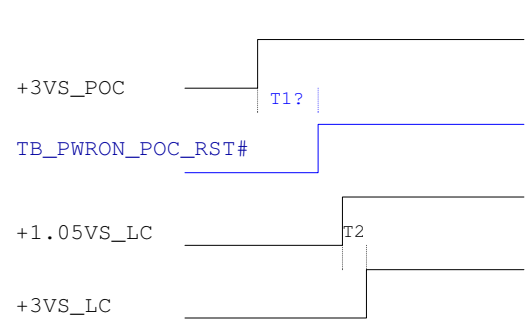
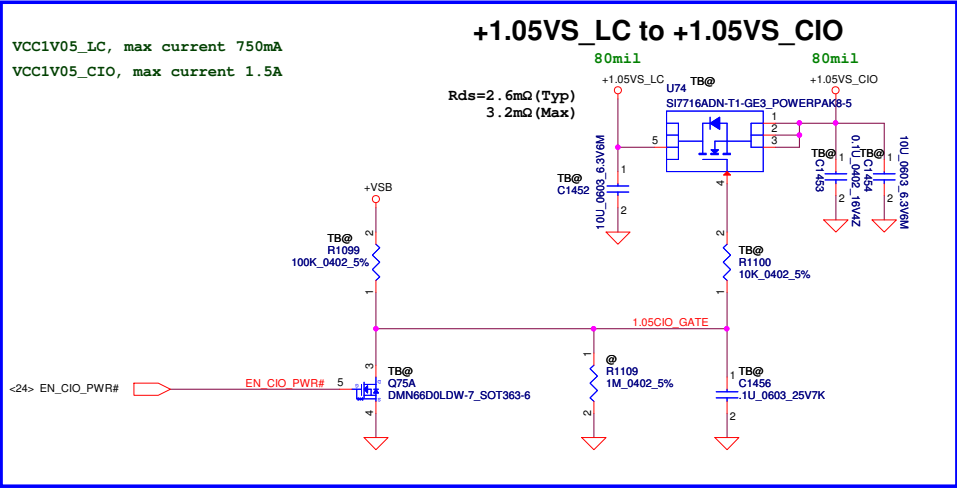
Size Std	Document Number	Rev
Custom	<b>Q3ZMC M/B LA-8481P Schematic</b>	1.0
Date:	Thursday, April 12, 2012	Sheet 24 of 51





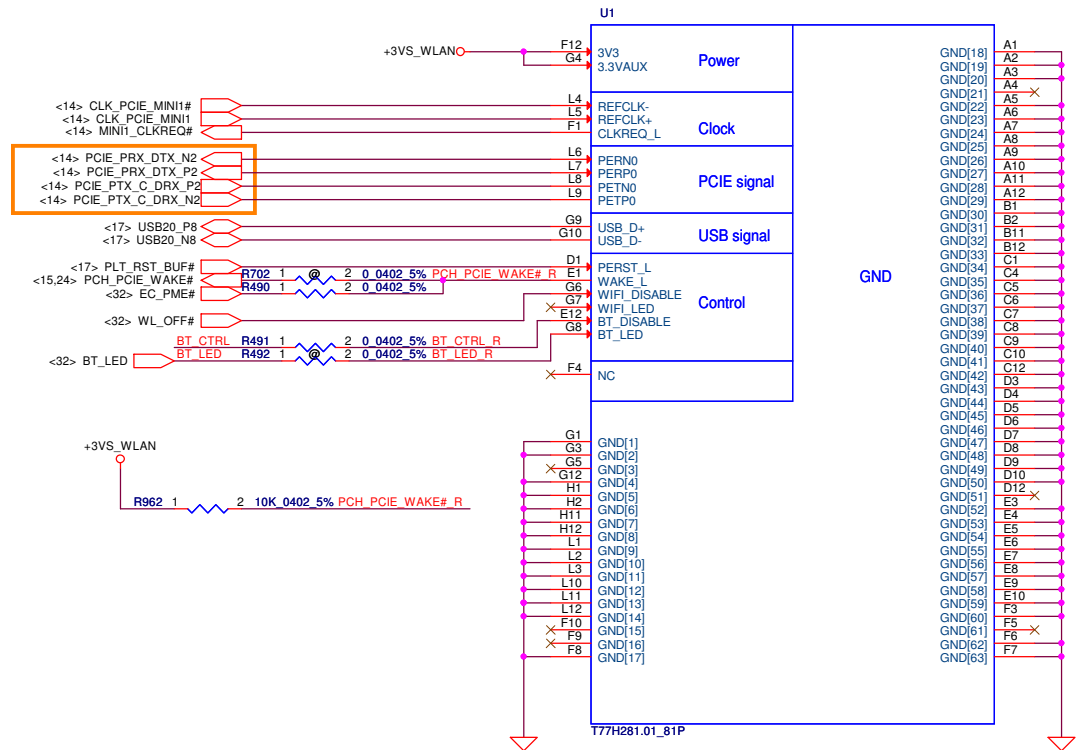
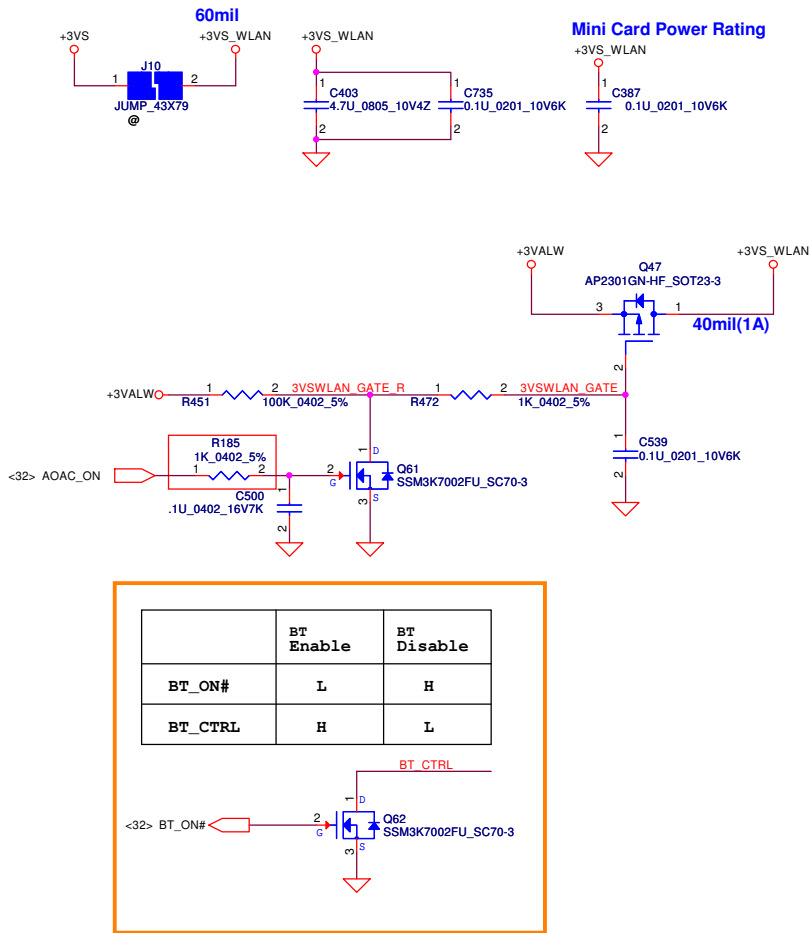


\_VCC1V05\_LC,max current 750mA  
\_VCC1V05\_CIO,max current 1.5A  
\_VCC3V3POC,max current 5mA  
\_VCC3V3\_LC,max current 350mA  
\_VCC\_DP@3V,max current 500mA  
\_VCC\_DP@12V,max current 0.8A  
in the case of 12V min power should be 10W

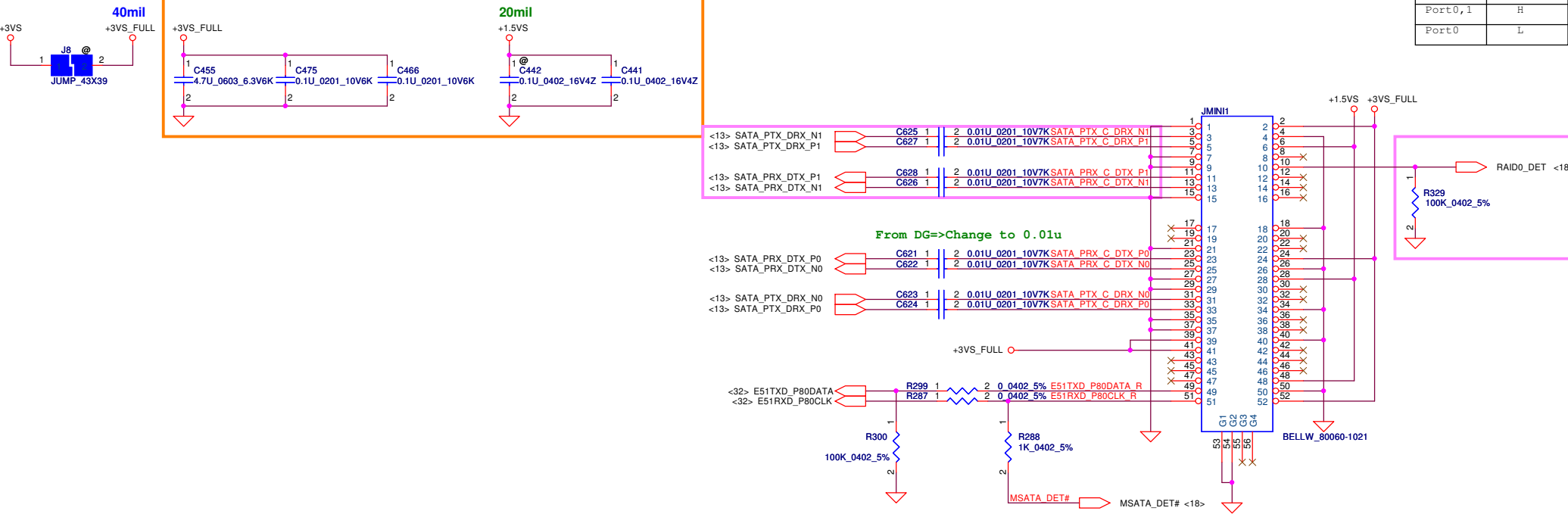


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				Q3ZMC M/B LA-8481P Schematic	1.0
				Date: Thursday, April 12, 2012	Sheet 27 of 51

# For Wireless LAN

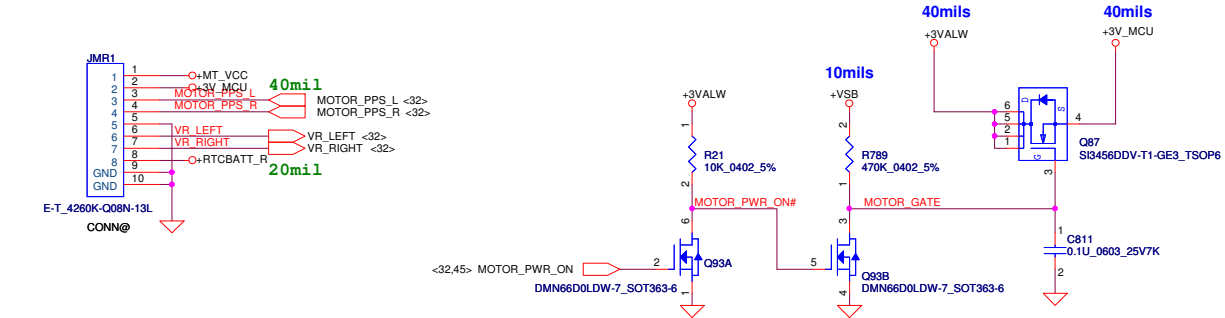


For mSATA

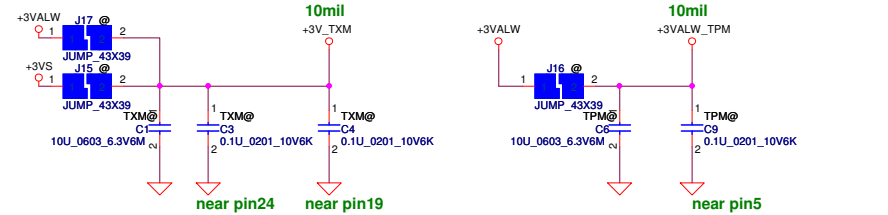


Function	RAIDO_DET
Port0,1	H
Port0	L

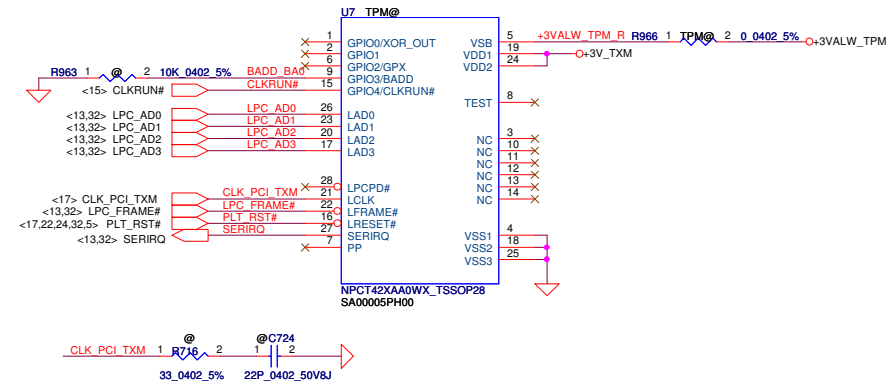
MOTOR/RTC

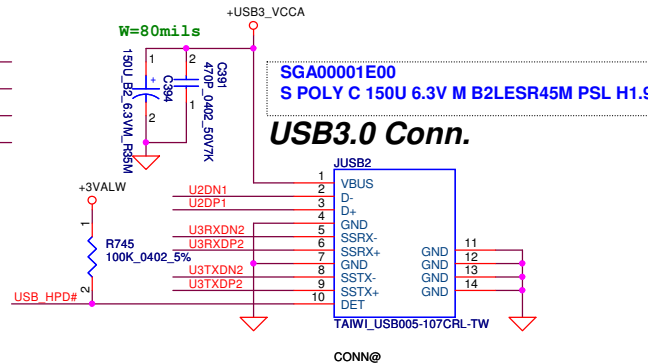
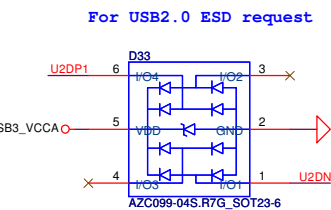
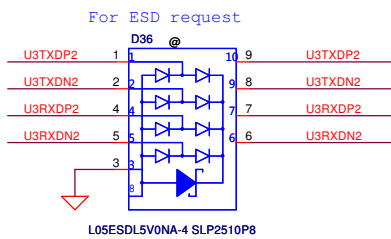
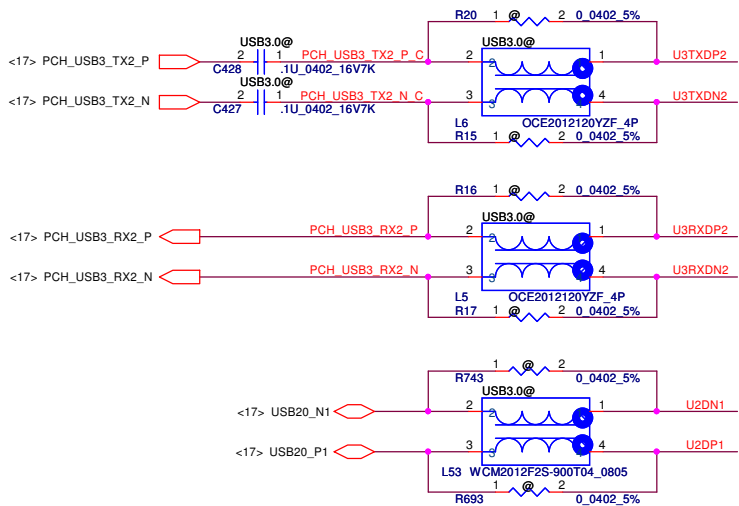
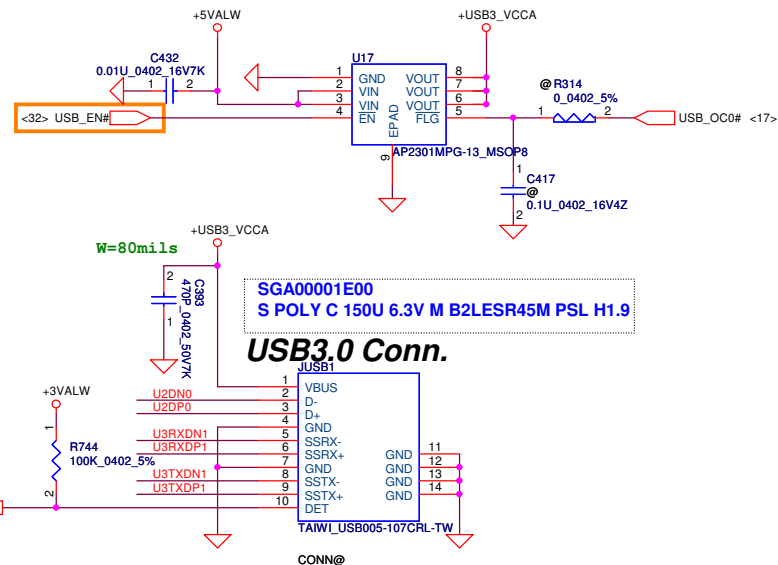
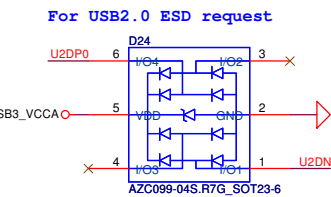
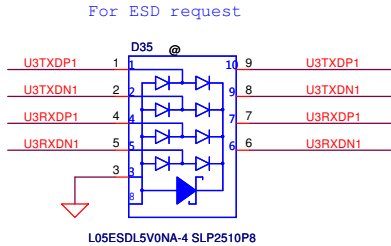
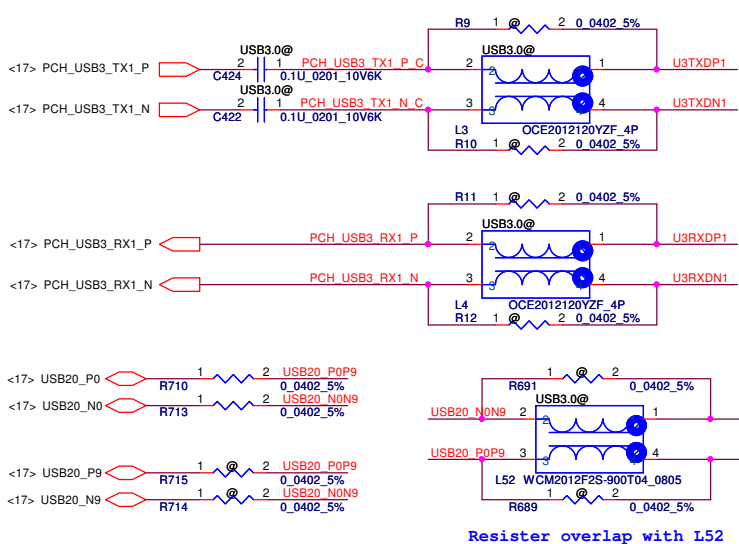


TPM

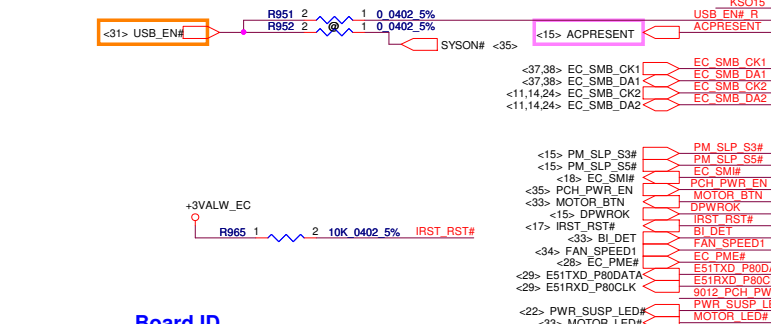
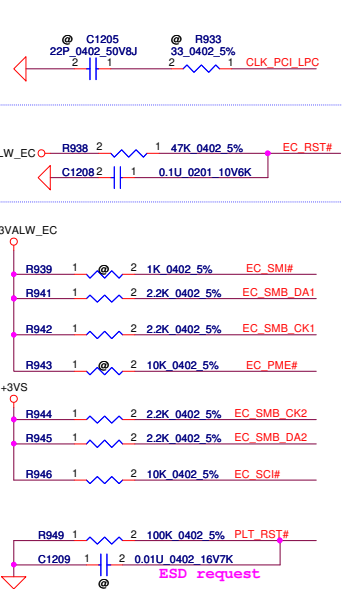


TPM -Address:  
Pin9 BADD  
1: 7Eh-7Fh (Default)  
0: EEh-EFh

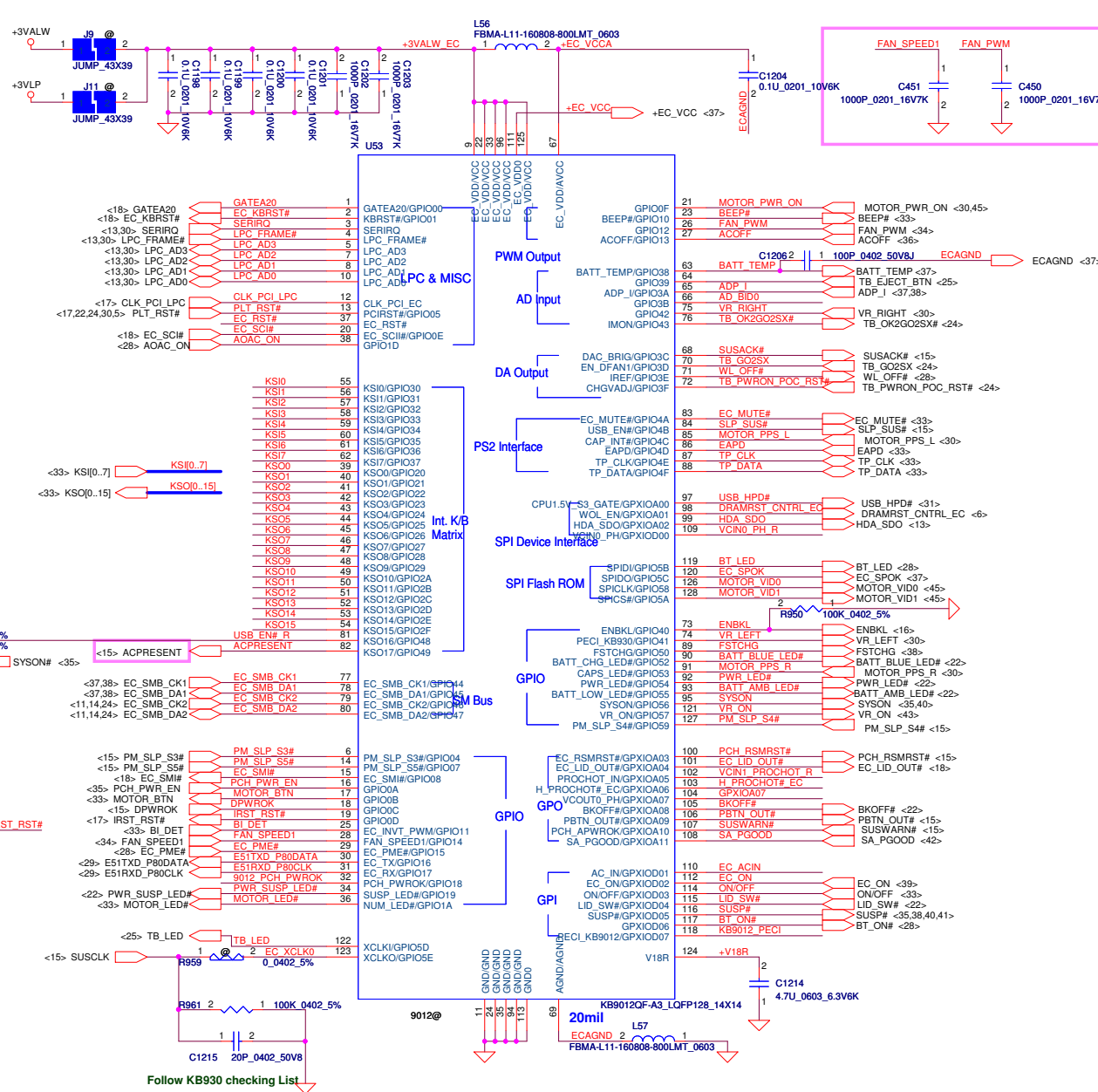
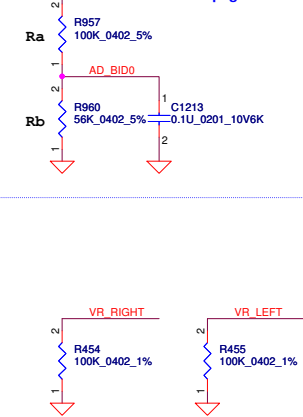




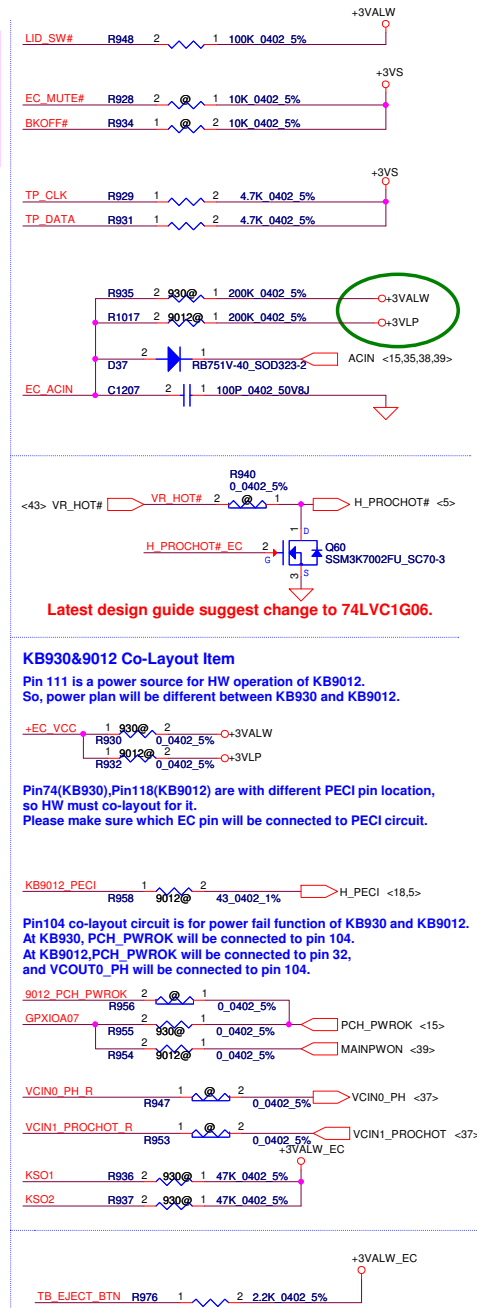
Security Classification		Compal Secret Data			
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				USB3.0	
Size	Custom	Document Number	Q3ZMC M/B LA-8481P Schematic		Rev 1.0
Date:	Thursday, April 12, 2012	Sheet	31	of	51



**Board ID**  
Analog Board ID definition,  
Please see page 3.



Follow KB930 checking List



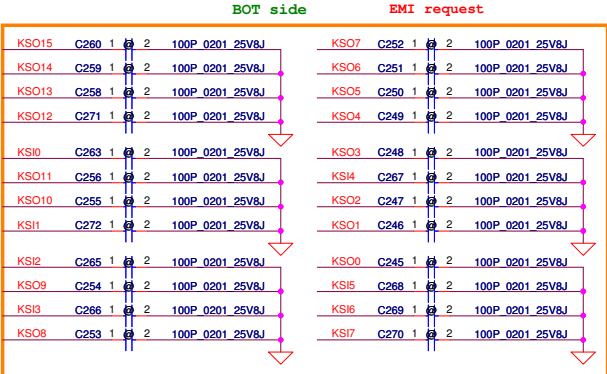
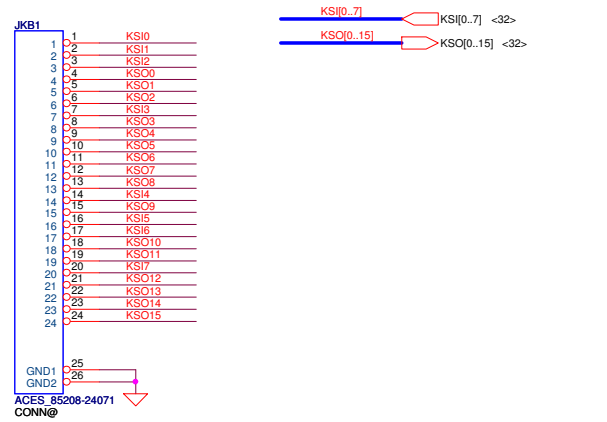
Latest design guide suggest change to 74LVC1G06.

**KB930&9012 Co-Layout Item**  
Pin 111 is a power source for HW operation of KB9012.  
So, power plan will be different between KB930 and KB9012.  
  
Pin74(KB930),Pin118(KB9012) are with different PECL pin location,  
so HW must co-layout for it.  
Please make sure which EC pin will be connected to PECL circuit.

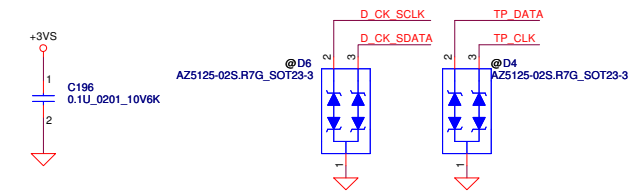
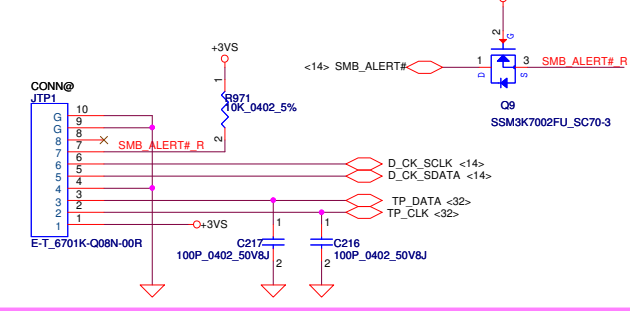
Pin104 co-layout circuit is for power fail function of KB930 and KB9012.  
At KB930, PCH\_PWROK will be connected to pin 104.  
At KB9012,PCH\_PWROK will be connected to pin 32,  
and VCOUT0\_PH will be connected to pin 104.

Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	EC ENE-KB930/KB9012		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc Number	Rev		
				Q3ZMC M/B LA-8481P Schematic	1.0		
				Date:	Thursday, April 12, 2012		
				Sheet	32 of 51		

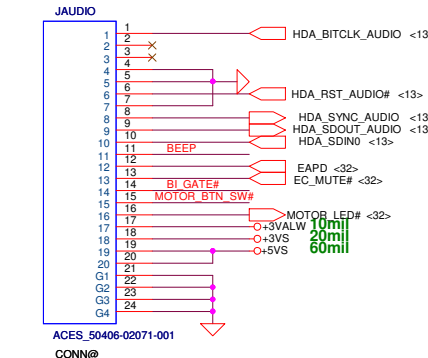
KB Conn.



TP Conn.

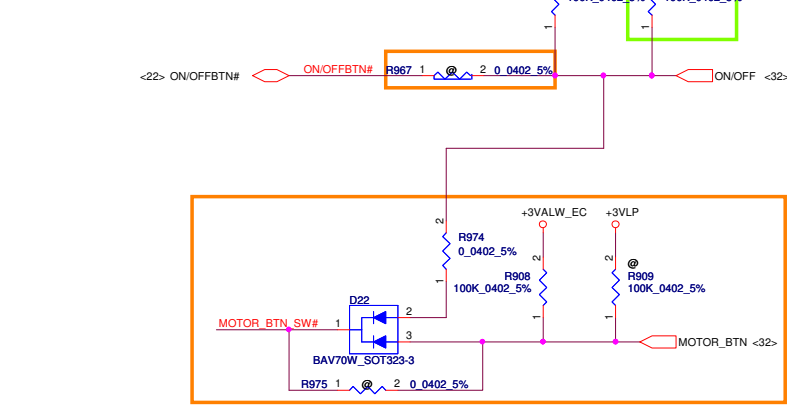


Audio/B 20pin

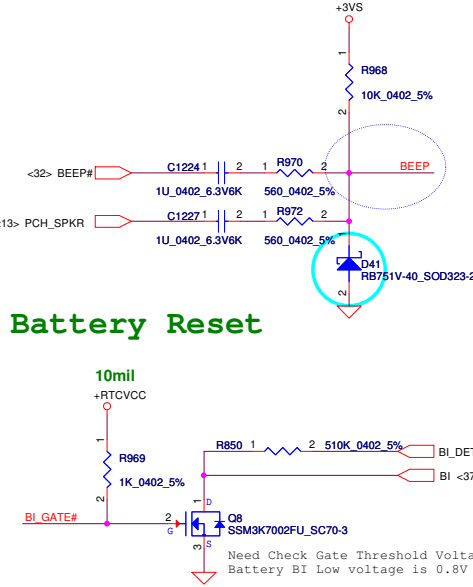


ON/OFF BTN

Motor BTN

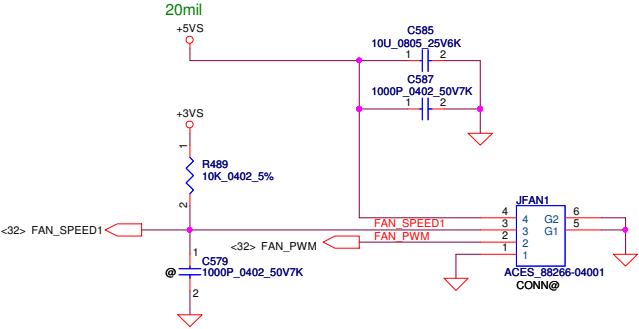


Battery Reset

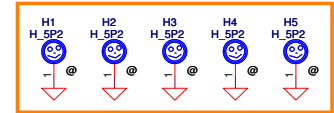


Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2012/4/6		Deciphered Date		2013/4/6		Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								BIOS, I/O Port & K/B Connector			
								Document Number		Rev	
								Q3ZMC M/B LA-8481P Schematic		1.0	
								Date: Thursday, April 12, 2012		Sheet 33 of 51	

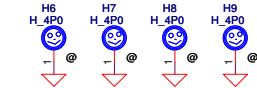
FAN Conn



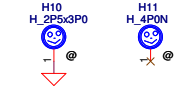
Stand-Off



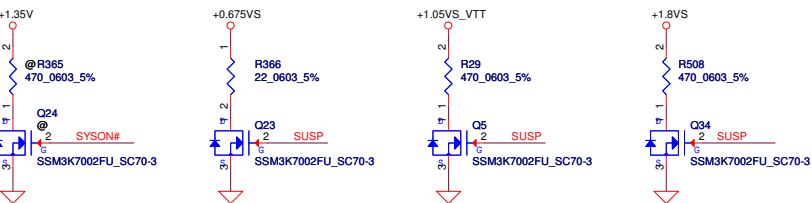
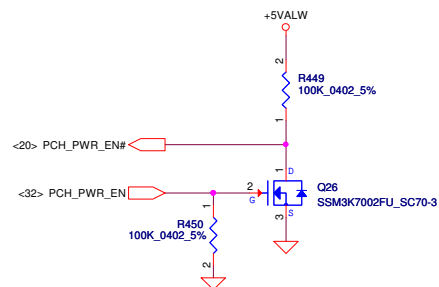
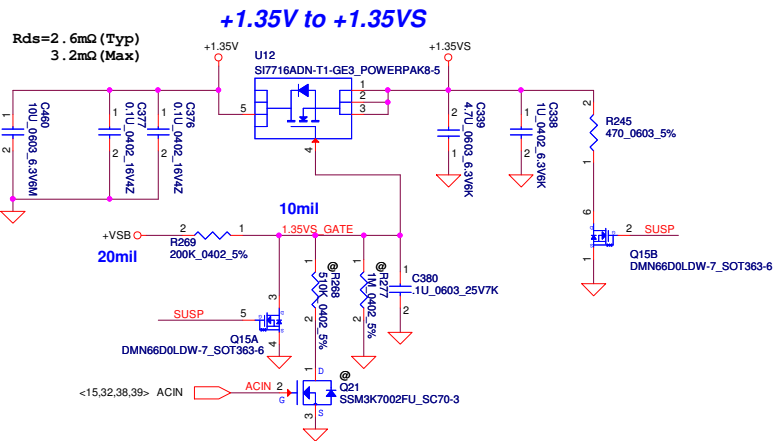
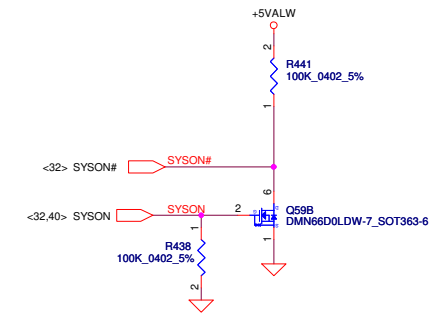
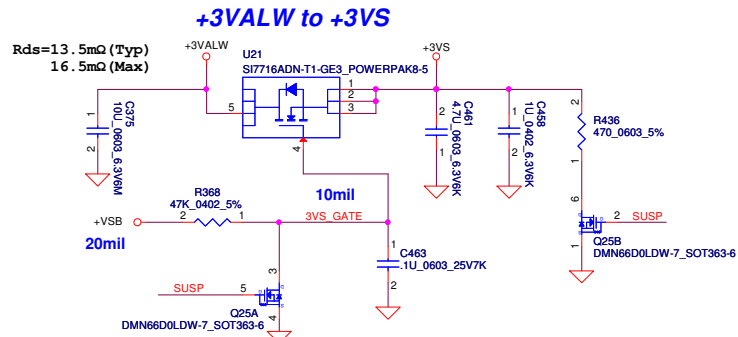
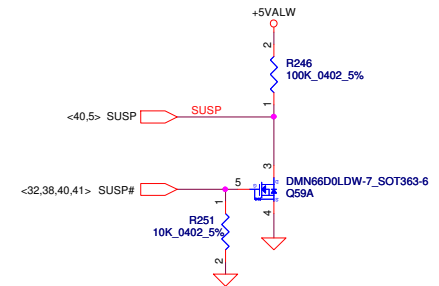
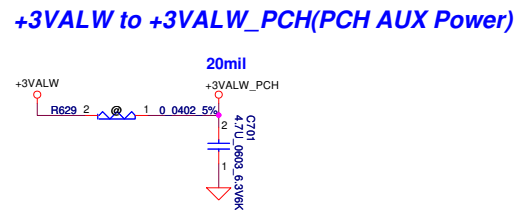
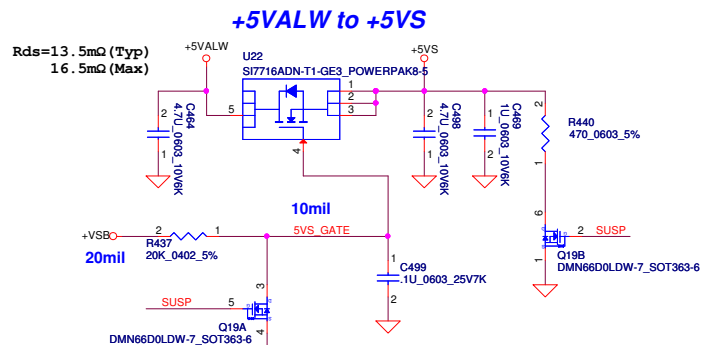
Thermal module



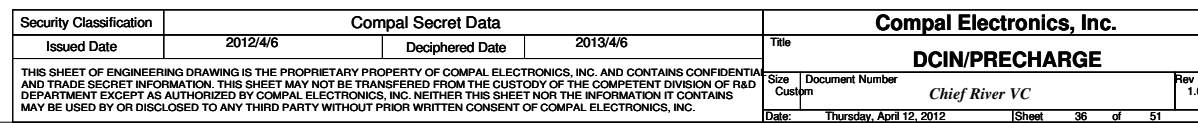
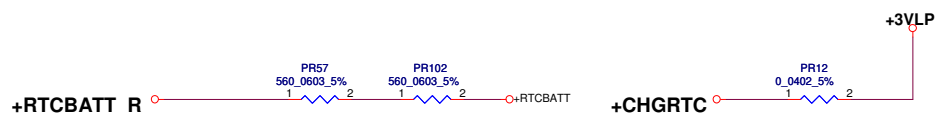
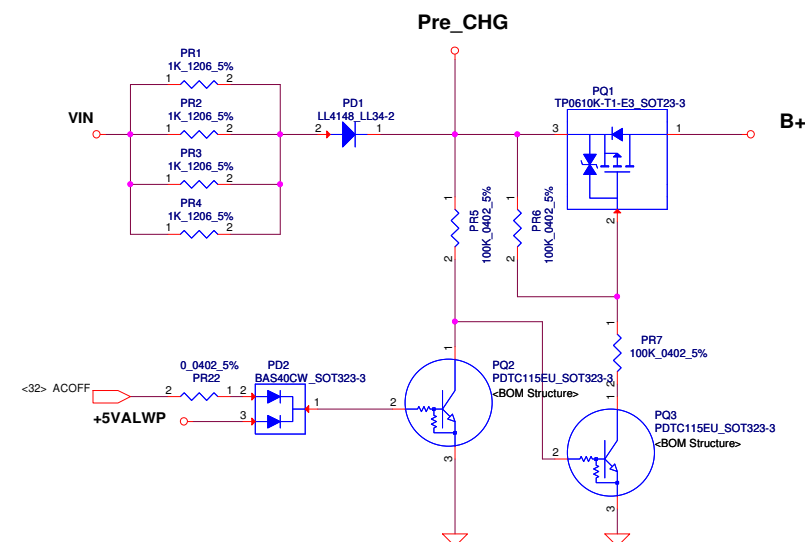
定位孔

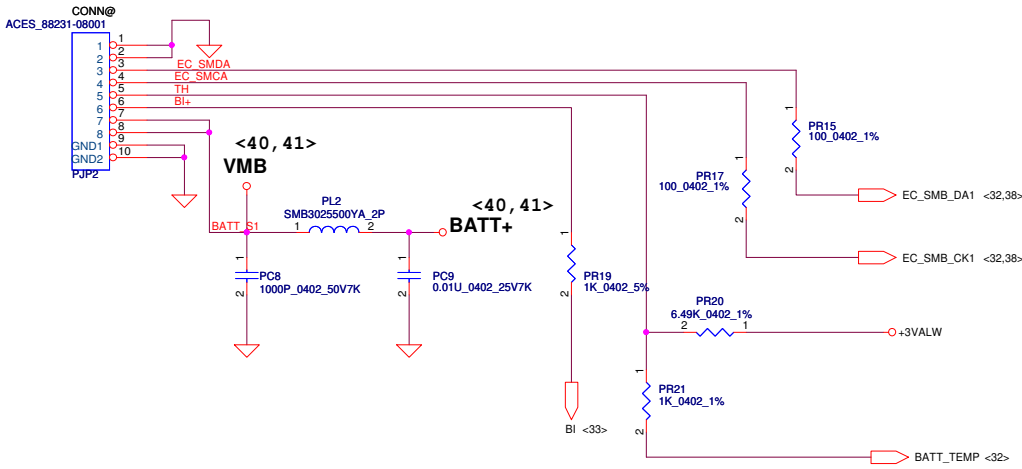


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	Step Motor, FAN, Screw Hole
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				Customer	1.0
				Date	Thursday, April 12, 2012
				Sheet	34 of 51



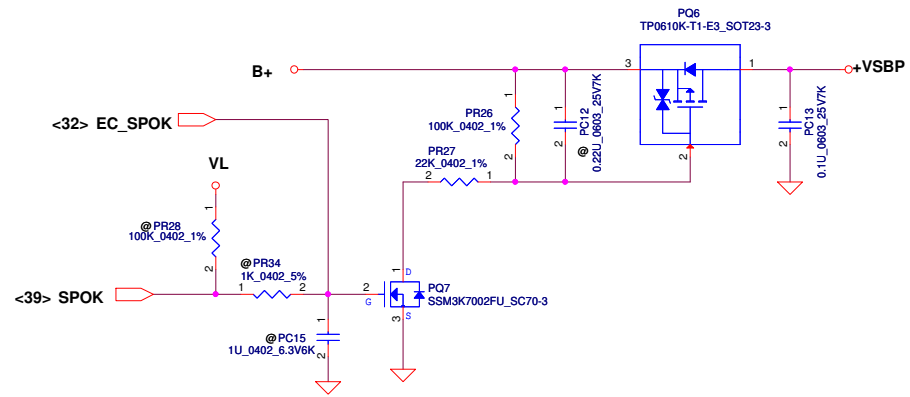
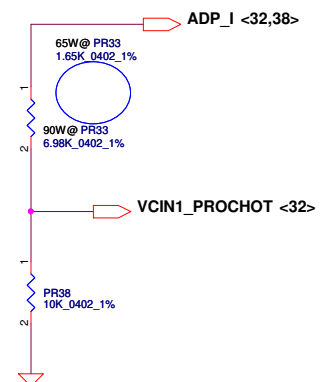
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2012/4/6		Deciphered Date		2013/4/6		Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						DC Interface					
						Document Number		Q3ZMC M/B LA-8481P Schematic		Rev 1.0	
						Date		Thursday, April 12, 2012		Sheet 35 of 51	
						Customer					
						Title					



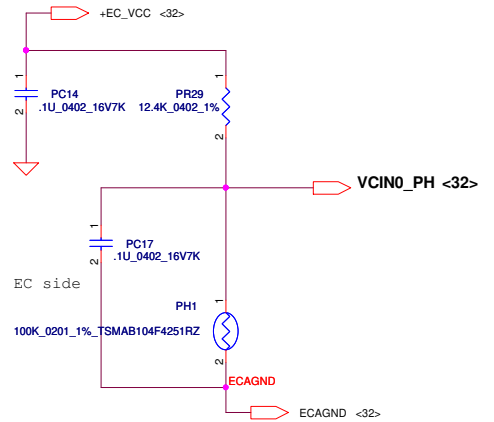


For 65W adapter==>action 70W , Recovery 54W  
 For 90W adapter==>action 97W , Recovery 75W  
 For 40W thunder bolt adapter==>action 50W , Recovery 38W  
 VCIN1=0.9V recover = 0.683V

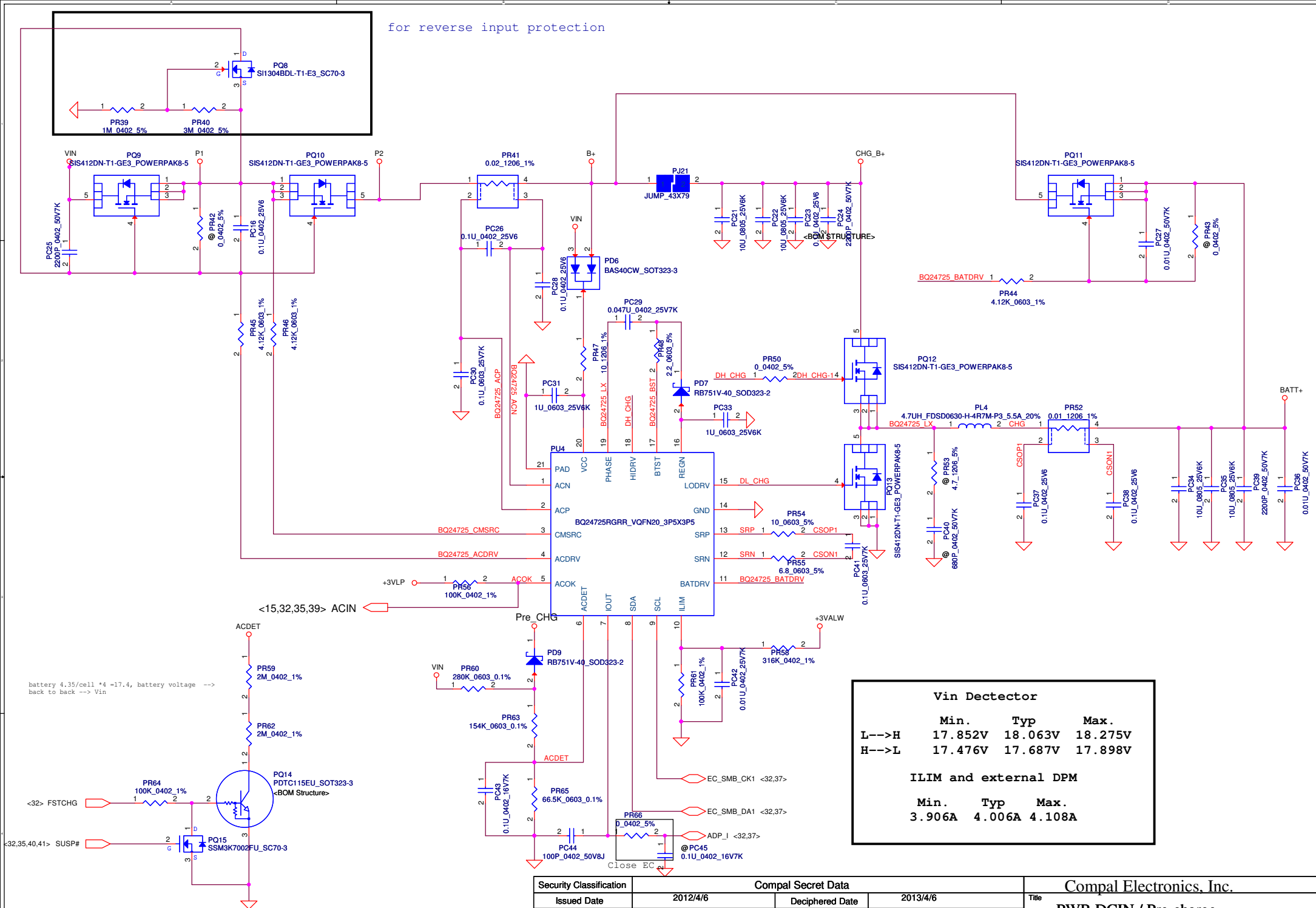
	G718	ENE9012
65W	3.92K	2.21K
90W	8.87K	6.98K
VCIN1	1.456V	1.2V
	1.148V	0.925V



PH1 under CPU botten side :  
 CPU thermal protection at 92 degree C for reference



for reverse input protection



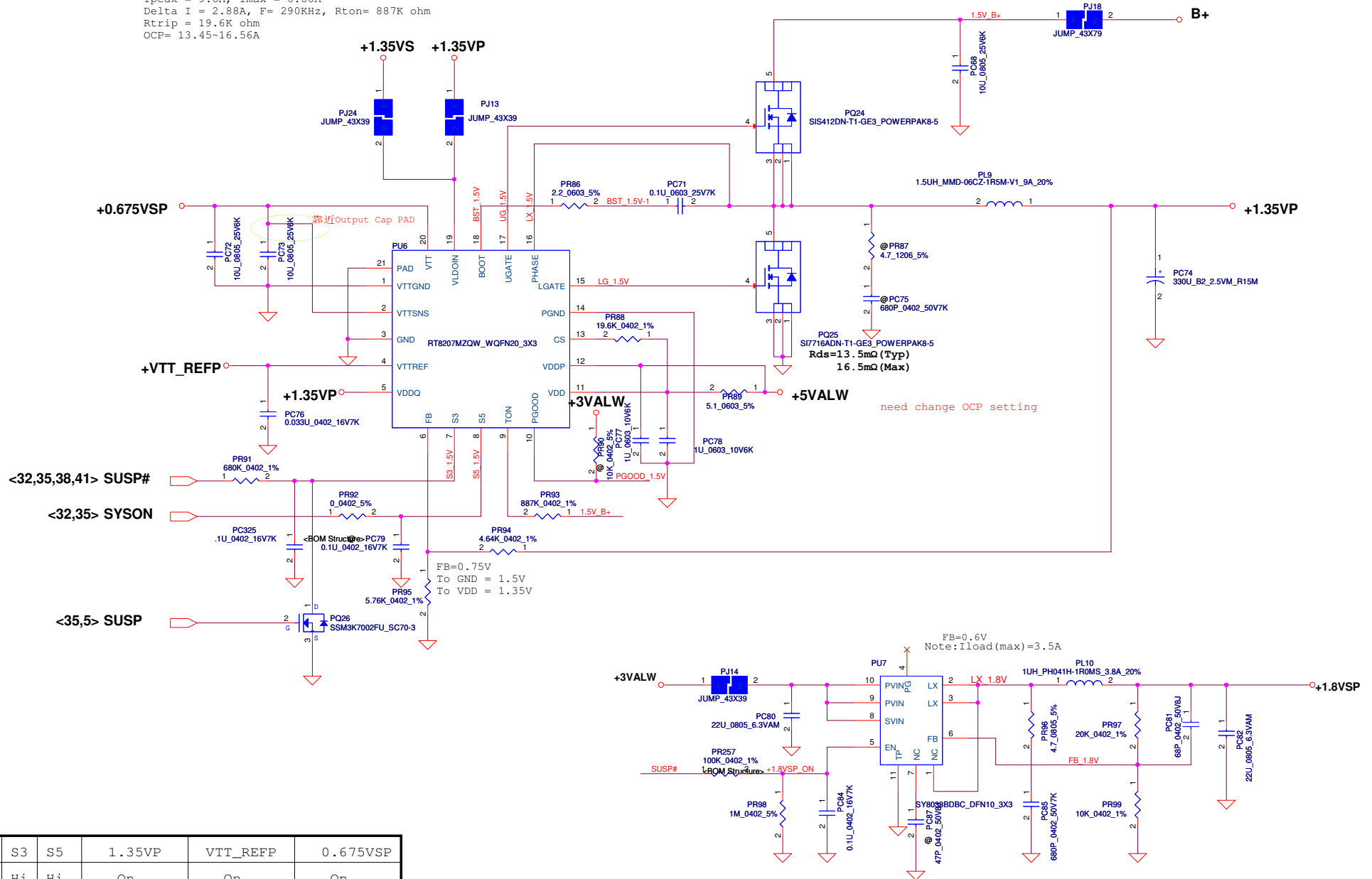
Security Classification			Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	PWR DCIN / Pre-charge		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev	
				Custom	Q3ZMC M/B LA-8481P Schematic	1.0	
				Date:	Thursday, April 12, 2012	Sheet	38 of 51

## ACIN



***Compal Electronics, Inc.***

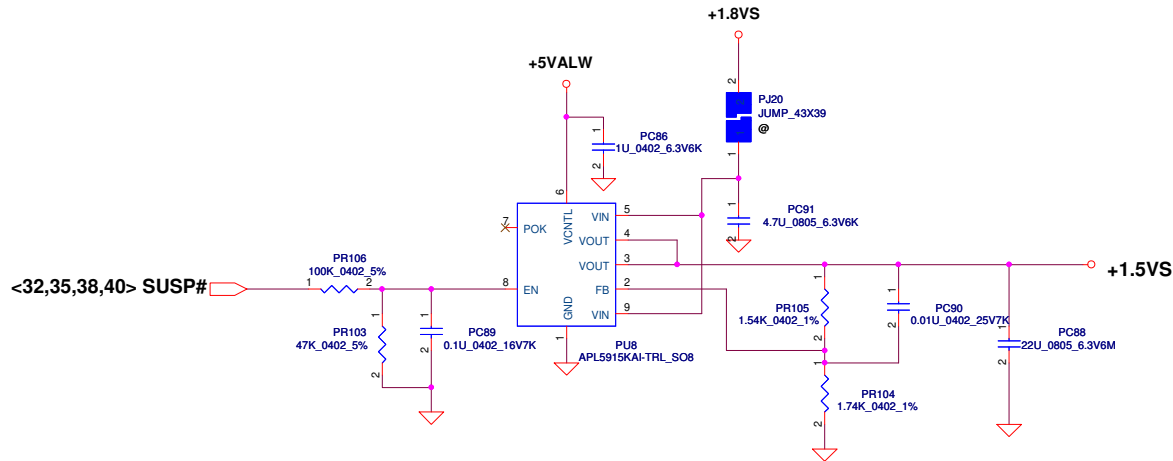
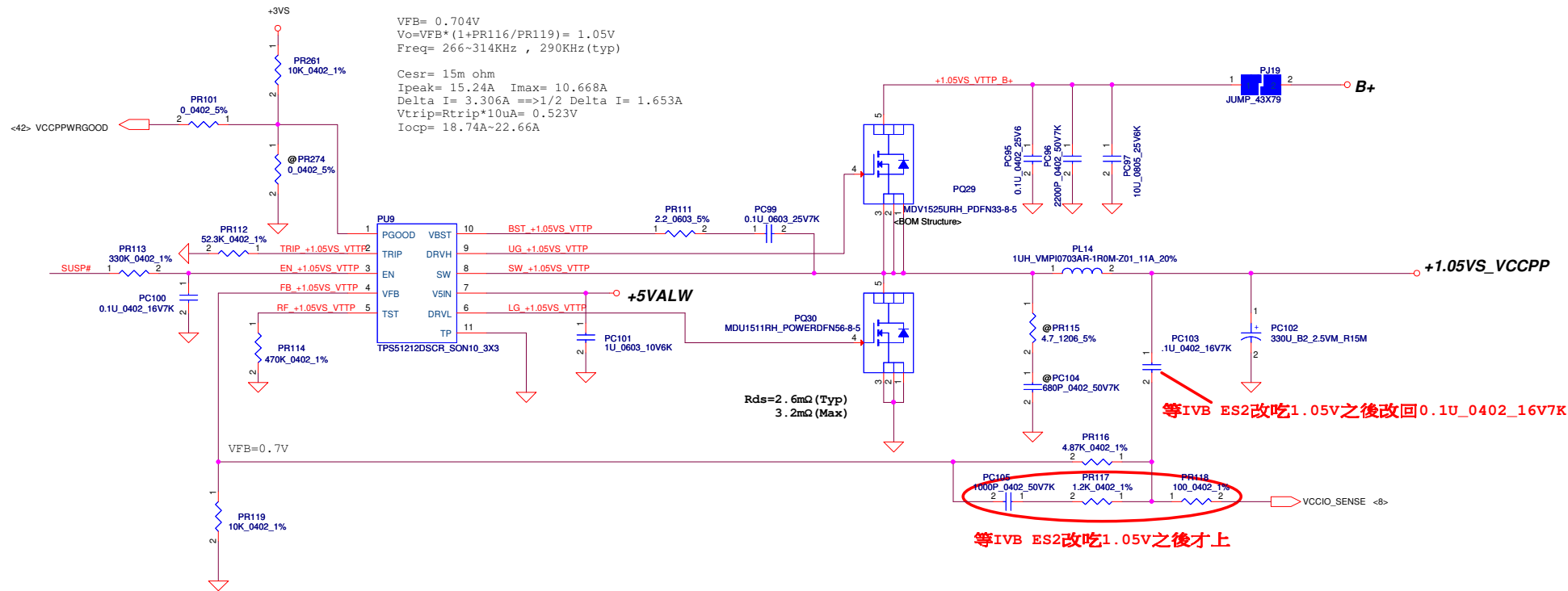
Ipeak = 9.8A, I<sub>max</sub> = 6.86A  
Delta I = 2.88A, F= 290KHz, R<sub>ton</sub>= 887K ohm  
R<sub>trip</sub> = 19.6K ohm  
OCP= 13.45~16.56A



STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off					

SY8033B enable pin without internal pull down, and  
RT8061or other 2nd source has 500K pull down resistor!So  
please review your application if  $R1 > 249K$  will cause  
enable pin logic high level is not enough

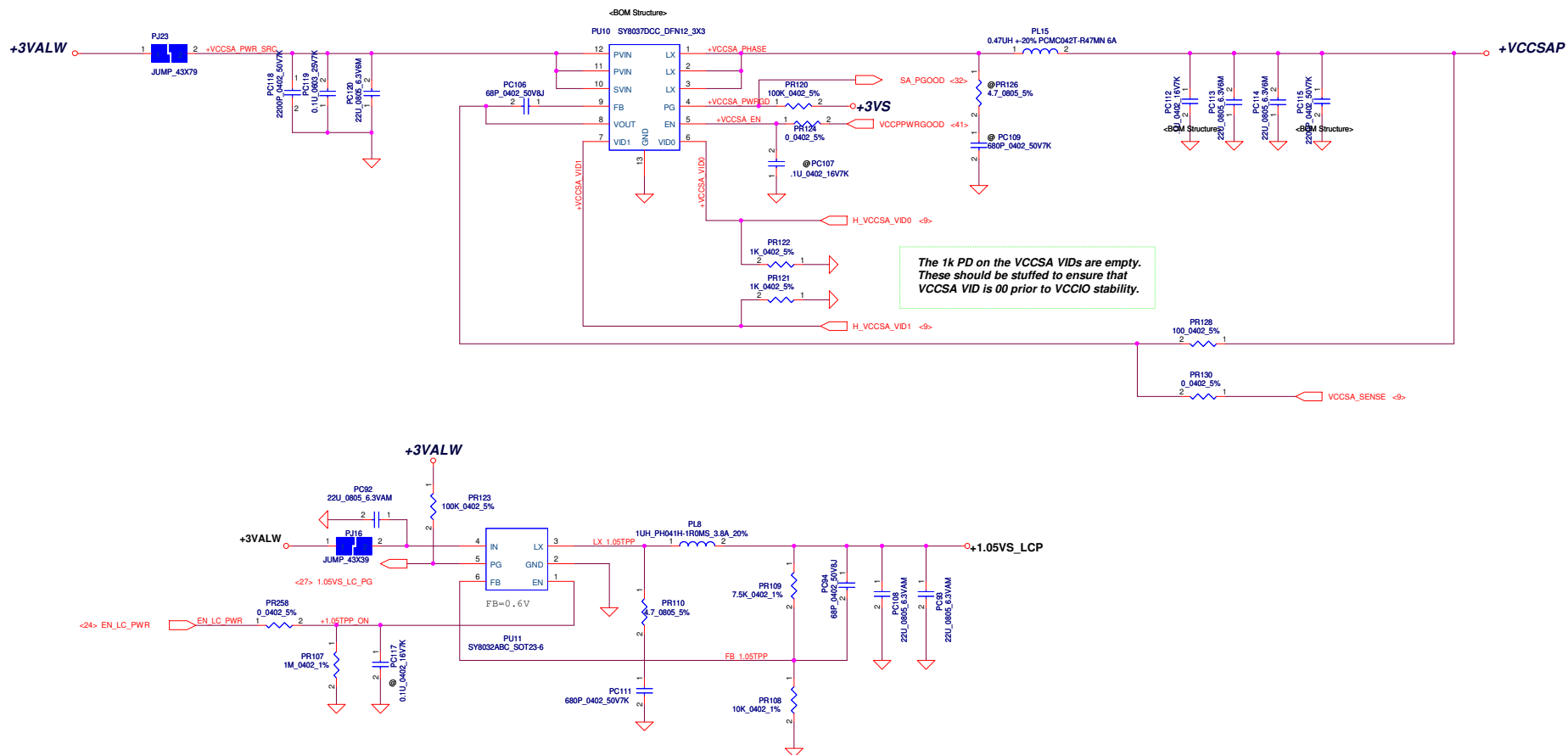
Security Classification		Compal Secret Data			
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title <b>1.5VP/0.75VSP/1.8VSP</b>	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number <i>Chief River VC</i>
				Date Thursday, April 12, 2012	Rev 1.0
				Sheet	40 of 51



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	+1.05VS_VTTP/+1.0VSP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Customer	Chief River VC
				Date	Thursday, April 12, 2012
				Sheet	41 of 51
				Rev	1.0

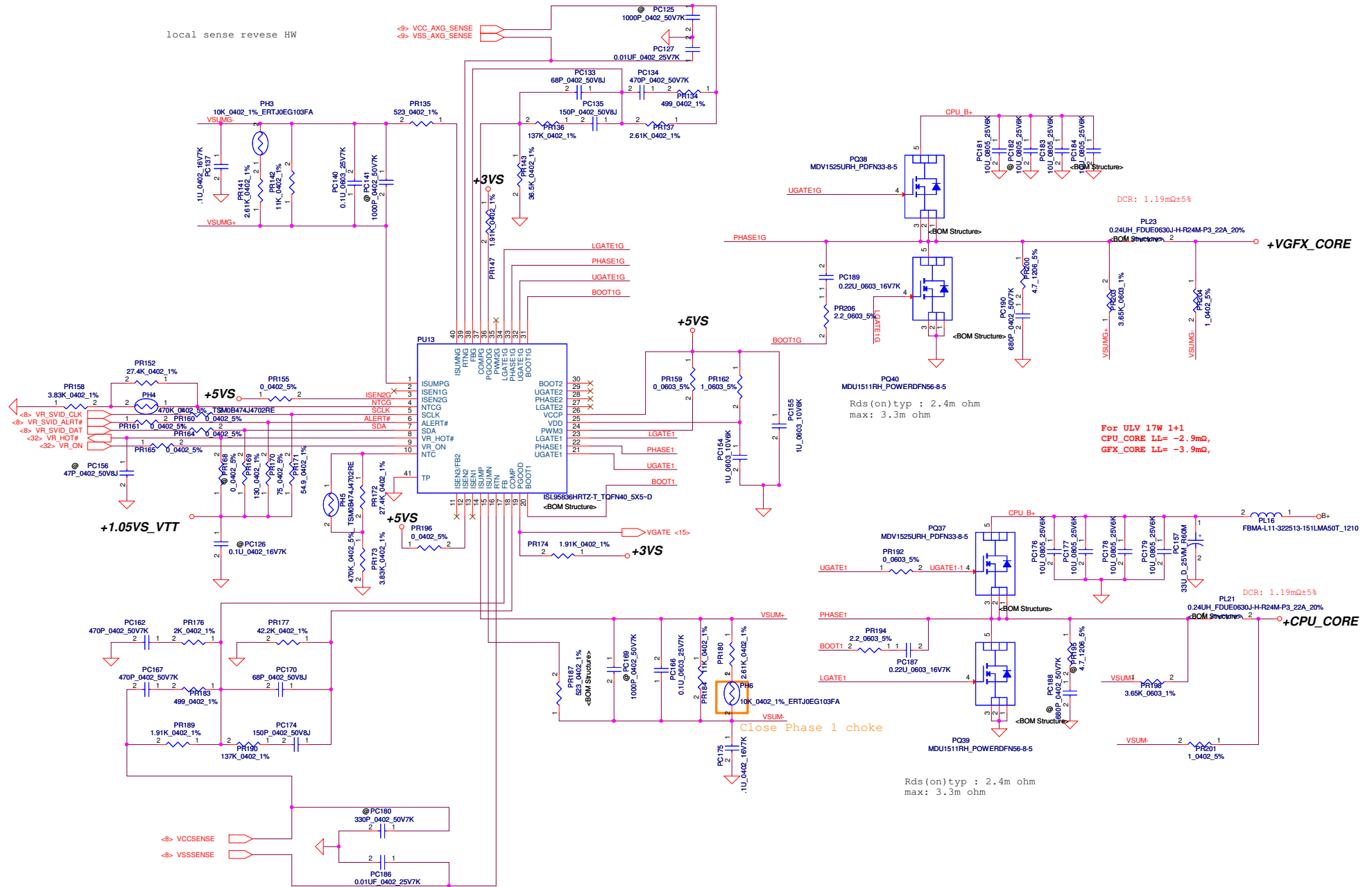
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



local sense reverse HW

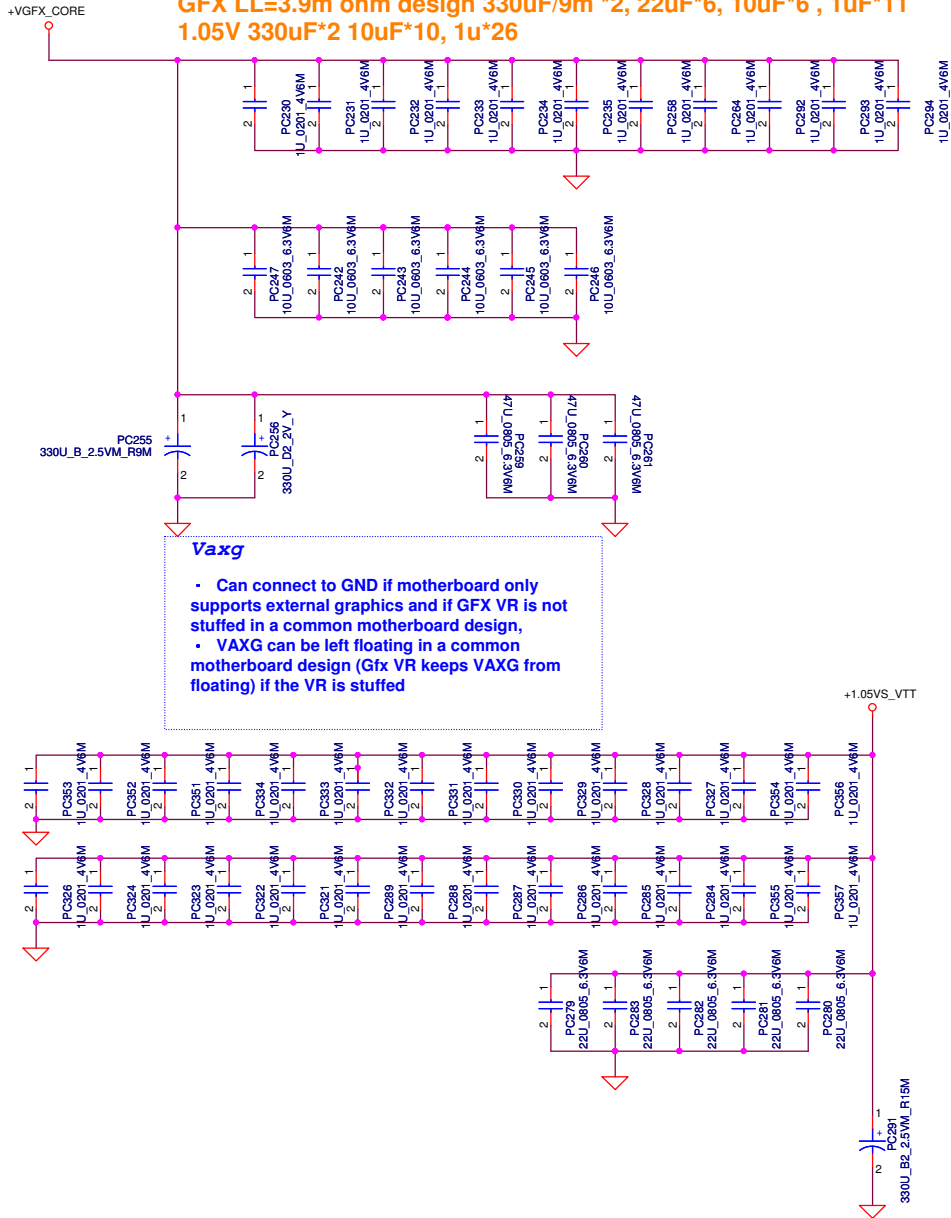
VCC\_AXG\_SENSE  
VSS\_AXG\_SENSE



local sense reverse HW

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	CPU CORE
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Chief River VC
				Date	Thursday, April 12, 2012
				Sheet	43 of 51

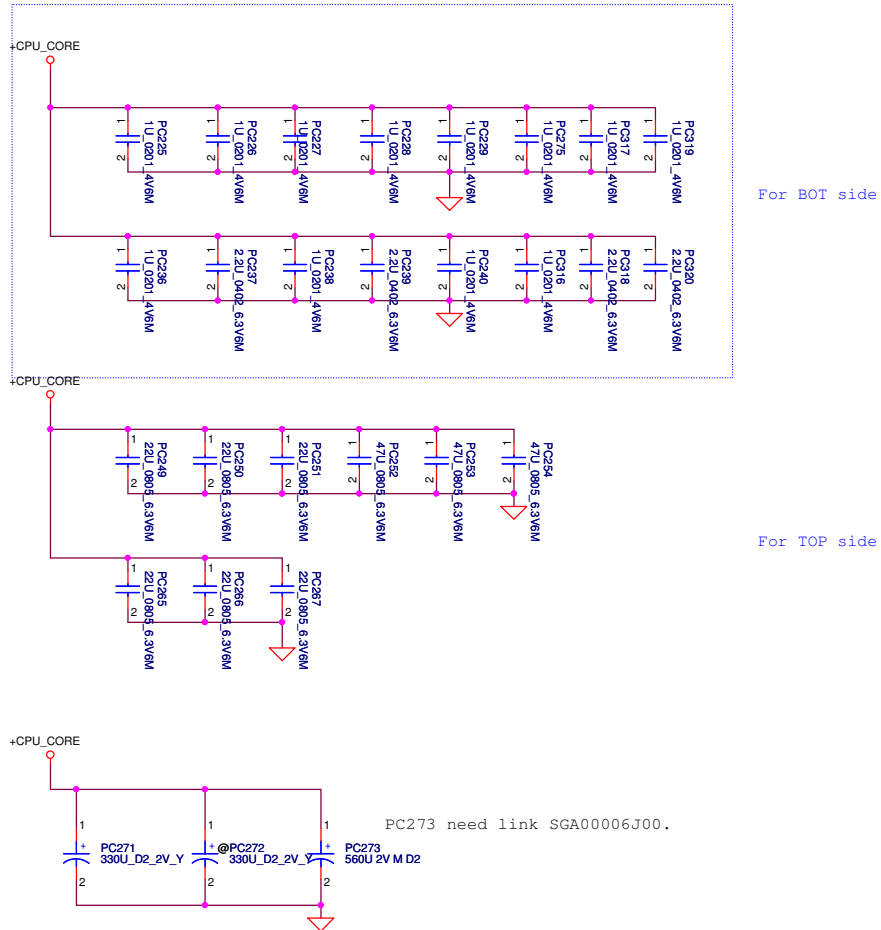
**PWR Rule**  
**CPU LL=2.9m ohm dedign 330uF/9m \*4, 22uF \*12, 2.2uF\*16**  
**GFX LL=3.9m ohm design 330uF/9m \*2, 22uF\*6, 10uF\*6, 1uF\*11**  
**1.05V 330uF\*2 10uF\*10, 1u\*26**



**Vauxg**

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

**INTEL Recommend**  
**3\*330uF(1 in other page),12\*22uF, 5 no stuff**  
**from PDDG 1.0**

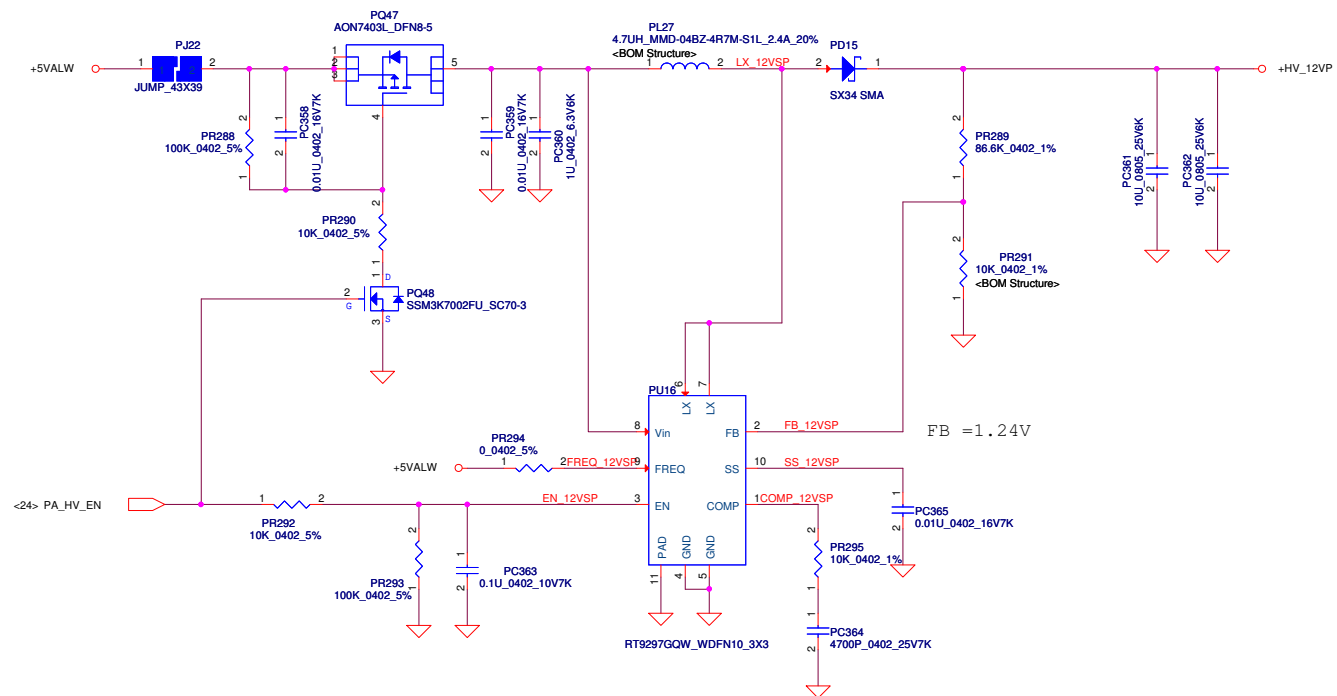


For BOT side

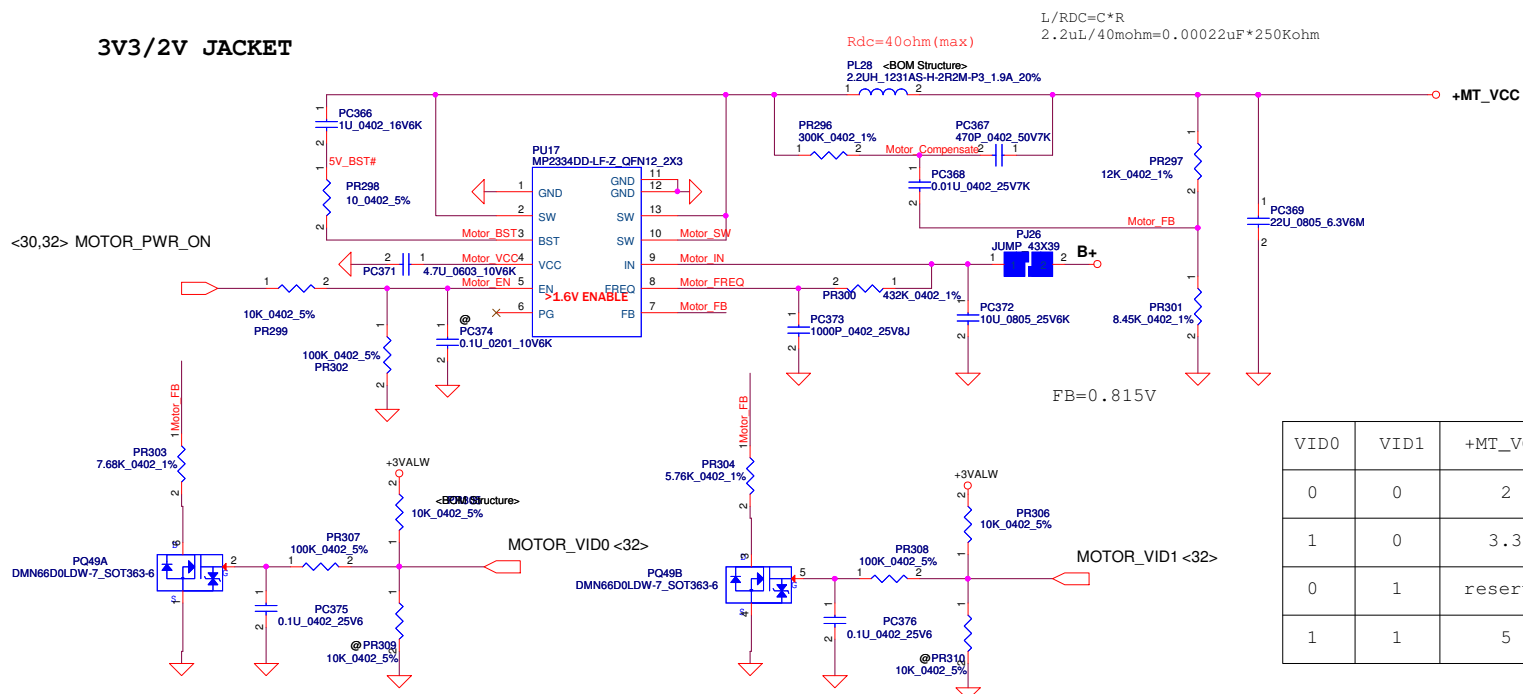
For TOP side

PC273 need link SGA00006J00.

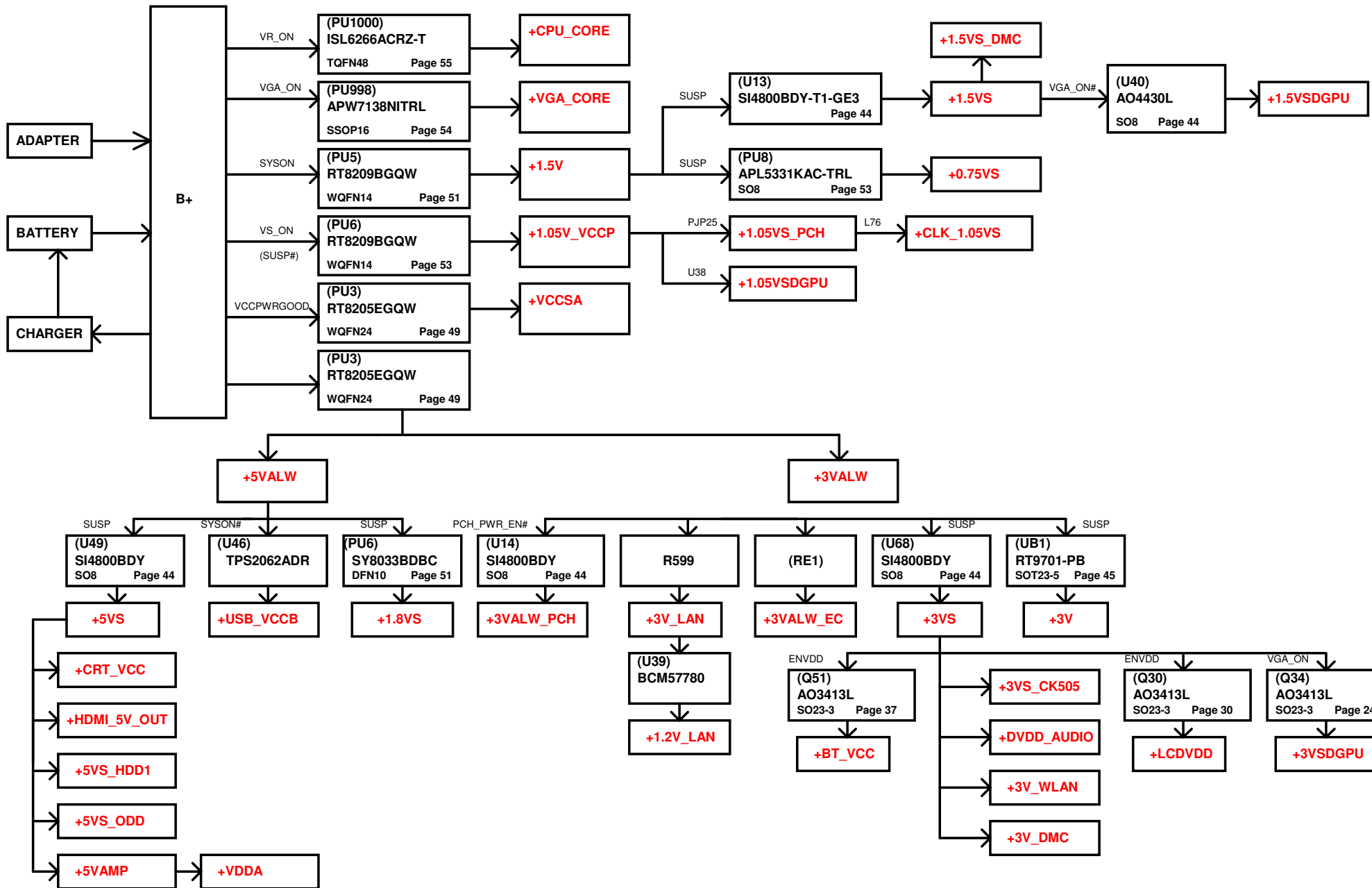
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	CPU CORE CAP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Chief River VC
				Date	Thursday, April 12, 2012
				Sheet	44 of 51
				Rev	1.0



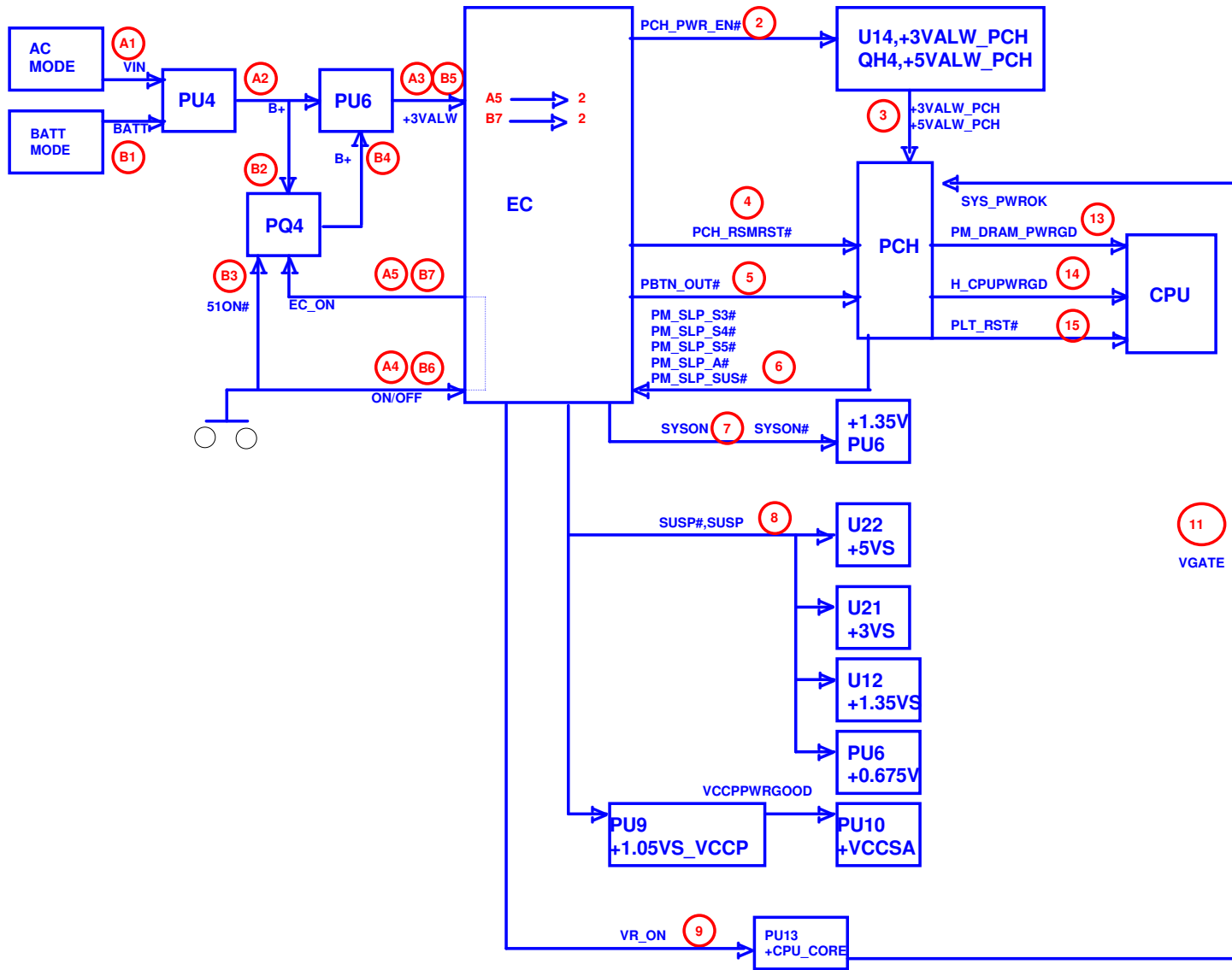
### 3V3/2V JACKET



VID0	VID1	+MT_VCC
0	0	2
1	0	3.3
0	1	reserve
1	1	5



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	Power Rail
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Q3ZMC M/B LA-8481P Schematic
				Date:	Thursday, April 12, 2012
				Sheet	46 of 51



## Version change list (P.I.R. List)

Page 1 of 2  
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Add ADP_ID circuit	Acer will add pull down resistor in adapter to detect ADP_ID.	0.1	36	Add PU1 SA003310280 (S IC LMV331IDCKRG4 SC70 5P COMPARATORS) Add PQ27 SB000009Q80 (S TR 2N7002KW 1N SOT323-3) Add PR13 PR16 SD034100280 (S RES 1/16W 10K +-1% 0402) Add PR14 SD034100380 (S RES 1/16W 100K +-1% 0402)	2011/12/05	EVT2
2	Add Jack_TEMP and PH1 circuit	Acer request add a thermistor on jack of DC in cable to protect jack.	0.1	37	Add PU3 SA000003K300 (S IC G718TMIU SOT23 8P OTP) Add PR30 SD000009R00 (S RES 1/16W 46.4K +-1% 0402) Add PR35 SD034953180 (S RES 1/16W 9.53K +-1% 0402) Add PR37 SD034232280 (S RES 1/16W 23.2K +-1% 0402) Del PR127 SD028000080 (S RES 1/16W 0 +-5% 0402)	2011/12/05	EVT2
3	Adjust 1.35V ocp setting and add boost resistor	Adjust 1.35V ocp setting Add boost resistor	0.1	40	Change PR88 to SD000003580 (S RES 1/16W 19.6K +-1% 0402) Change PR86 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	2011/12/05	EVT2
4	Add 1.05V boost resistor and adjust output voltage Change choke to 1uH	Add 1.05V boost resistor and adjust output voltage Change choke to 1uH for efficiency of heavy load	0.1	41	Change PR111 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603) Change PR116 to SD034487100 (S RES 1/16W 4.87K +-1% 0402 (LF)) Change PL14 to SH00000KS00 (S COIL 1UH +-20% VMI0703AR-1R0M-201 11A)	2011/12/05	EVT2
5	Adjust GFX frequency	Adjust GFX frequency to 400kHz for reduce ripple	0.1	43	Change PR143 to SD034365280 (S RES 1/16W 36.5K +-1% 0402)	2011/12/05	EVT2
6	Adjust CPU output cap	Adjust CPU output cap for transient	0.1	44	Change PC273 to SGA00006J00 (S POLY C 560U 2V M D2 LESR4.5M SX H1.9) unpop PC272 SGA20331E10 (S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9)	2011/12/05	EVT2
7	Adjust 0.675V enable timing	Adjust 0.675V enable timing	0.1	40	Change PC325 to SE076104K80 (S CER CAP .1U 16V K X7R 0402)	2011/12/05	EVT2
8	Adjust 1.05VS_LCP sequence	Change 1.05VS_LCP from APL5930 to SY8032 for thoundbolt sequence.	0.2	42	Change PU11 to SA000055100 (S IC SY8032ABC SOT23 6P PWM) Change PR107 to SD034100480 (S RES 1/16W 1M +-1% 0402) Add PL8 to SH00000MN00 (S COIL 1UH +-20% PH041H-1R0MS 3.8A) Add PR110 to SD002470B80 (S RES 1/8W 4.7 +-5% 0805) Change PC111 to SE074681K80 (S CER CAP 680P 50V K X7R 0402) Change PC92 to SE000008180 (S CER CAP 22U 6.3V M XES 0805 H1.25) Add PR123 to SD028100380 (S RES 1/16W 100K +-5% 0402) Change PR108 to SD034100280 (S RES 1/16W 10K +-1% 0402) Change PR109 to SD034750180 (S RES 1/16W 7.5K +-1% 0402) Change PC94 to SE071680J80 (S CER CAP 68P 50V J NPO 0402)	2012/01/05	DVT
9							
10	add boost resistor	add Charger boost resistor	0.2	38	Change PR48 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	2012/01/05	DVT
11	add boost resistor	add 3V5V boost resistor	0.2	39	Change PR73 and PR74 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	2012/01/05	DVT
12	add boost resistor	add CPU and GFX boost resistor	0.2	43	Change PR194 and PR206 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	2012/01/05	DVT
13	Change main source	Change main source for reduce component kind	0.2	39	Change PL7 to SH00000MB00 (S COIL 4.7UH +-20% FSDSD0630-H-4R7M=P3 5.5A (7*7*3))	2012/01/05	DVT
14	Adjust Jack_TEMP resistor	Adjust Jack_TEMP resistor, because PCCP change thermistor to 0603 size (TSM1A104F4361RZ)	0.2	37	change PR30 to SD034442280 (S RES 1/16W 44.2K +-1% 0402) change PR37 to SD034215280 (S RES 1/16W 21.5K +-1% 0402)	2012/01/05	DVT
15	Add ADP_ID circuit	Add ADP_ID circuit(65W)	0.2	36	Add PR23 to SD028000080 (S RES 1/16W 0 +-5% 0402) change PR16 to SD034270280 (S RES 1/16W 27K +-1% 0402) Add PC142 to SE074102K80 (S CER CAP 1000P 50V K X7R 0402)	2012/01/05	DVT
16	Change main source	Change main source for 不完全替代 with HW	0.2		change P07,P026,P015,P027,P048 from SB000009Q80 to SB000009610 (S TR SSM3K7002FU 1N SC70-3)	2012/01/31	DVT
17							

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	PIR (PWR)
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	Q3ZMC M/B LA-8481P Schematic
				Date	Thursday, April 12, 2012
				Sheet	48 of 51

## Version change list (P.I.R. List)

Page 2 of 2  
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
18	Del ADP_ID circuit	Acer will change adapter type to 音叉式 from PoGo, so del ADP_ID circuit.	0.3	36	Del PU1 SA003310280 (S IC LMV331IDCKRG4 SC70 5P COMPARATORS) Del PQ27 SB000009Q80(S TR 2N7002KW 1N SOT323-3) Del PR13 SD034100280(S RES 1/16W 10K +-1% 0402) Del PR14 SD034100380(S RES 1/16W 100K +-1% 0402) Del PR23 to SD0280000080(S RES 1/16W 0 +-5% 0402) Del PR16 to SD034270280(S RES 1/16W 27K +-1% 0402) Del PC142 to SE074102K80(S CER CAP 1000P 50V K X7R 0402)	2012/03/13	PVT
19					Del PU3 SA000003K300 (S IC G718TMIU SOT23 8P OTP) Del PR30 to SD034442280(S RES 1/16W .44.2K +-1% 0402) Del PR35 SD034953180(S RES 1/16W 9.53K +-1% 0402) Del PR37 to SD034215280(S RES 1/16W 21.5K +-1% 0402) Add PC17 SE076104K80(S CER CAP .1U 16V K X7R 0402) Change PR29 to SD00000AJ80(S RES 1/16W 12.4K +-1% 0402)		
20	Del jack_temp circuit	Acer will change adapter type to 音叉式 from PoGo, so del jack_temp protect circuit.	0.3	37		2012/03/13	PVT
21	SPOK change to EC_SPOK	For reduce power consumption of DS3, so close +VSB power in DS3, DS4, DS5.	0.3	37	Del PR28 SD034100380(S RES 1/16W 100K +-1% 0402) Del PR34 SD028100180(S RES 1/16W 1K +-5% 0402) Del PC15 SE000000K80(S CER CAP 1U 6.3V K X5R 0402)	2012/03/13	PVT
22	change VCCSA IC version	SY8037C IC version change to SY8037D for accord with intel VCCSA spec.	0.3	42	Change PU10 to SA000050000(S IC SY8037DDCC DFN 12P PWM)	2012/03/13	PVT
23	Add snubber	Add snubber of GFX by hw request.	0.3	43	Add PR200 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC190 SE074681K80(S CER CAP 680P 50V K X7R 0402)	2012/03/13	PVT
24	Add MOTOR POWER	HW change motor power solution to PWM.	0.3	45	Add PU17 SA00005NY00(S IC MP2334DD-LF-Z QFN 12P PWM) Add PL28 SH00000N000(S COIL 2.2UH +-20% 1231AS-H-2R2M=P3 1.9A) Add PC366 SE000000U00(S CER CAP 1U 16V K X5R 0402) Add PC367 SE074471K80(S CER CAP 470P 50V K X7R 0402) Add PC368 SE075103K80(S CER CAP .01U 25V K X7R 0402) Add PC369, PC371 SE00000MA00(S CER CAP 4.7U 10V K X5R 0603) Add PC372 SE00000QK00(S CER CAP 10U 25V K X5R 0805 H1.25) Add PC373 SE068102J80(S CER CAP 1000P 25V J NPO 0402) Add PC375, PC376 SE00000G880(S CER CAP 0.1U 25V K X5R 0402) Add PR296 SD034300380(S RES 1/16W 300K +-1% 0402) Add PR297 SD034120280(S RES 1/16W 12K +-1% 0402) Add PR298 SD028100A00(S RES 1/16W 10 +-5% 0402) Add PR300 SD034432380(S RES 1/16W 432K +-1% 0402) Add PR301 SD000000680(S RES 1/16W 8.45K +-1% 0402) Add PR302, PR307, PR308 SD028100380(S RES 1/16W 100K +-5% 0402) Add PR303 SD000002300(S RES 1/16W 7.68K +-1% 0402) Add PR304 SD034576180(S RES 1/16W 5.76K +-1% 0402) Add PR299, PR305, PR306 SD028100280(S RES 1/16W 10K +-5% 0402) Add PQ49 SB00000DH00(S TR DMN66D0LDW-7 2N SOT363-6)	2012/03/13	PVT
25							
26							
27							
28	Adjust HW throttling point	Because thunder bolt adapter is 40W, OCP 130% adjust HW throttling to 125% 50W recover point 38W	0.3	37	Change PR33 to SD034165180(S RES 1/16W 1.65K +-1% 0402)	2012/03/13	PVT
29							
30							
31							
32							
33							
34							

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	PIR (PWR)
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number Q3ZMC M/B LA-8481P Schematic
Date: Thursday, April 12, 2012				Sheet	49 of 51

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
0919(In Layout)							
1.Update R,C 0201,0402,0603,0805,1206 PCB footprint to small size					0928	1013	
2.Swap DDR Data BUS					1.Change RTC cap from 1U 0603 to 1U 0402:C502,C516	1.Add Step Motor circuit	
					2.Remove FAN some parts:R753,C788,D51,D52	2.On Board iSSD:i100 change to mSATA SSD	
					3.Change USB connector foot print to TAIWI_USB005-107CRL-TW_10P-T	3.WLAN change to on board:MD225	
					4.Change C196,C387,C735,C102 to 0.1uF_0201_10V6K:SE00000SV00	4.Change Card Reader	
					5.Remove L2	PCIE from Port4 to Port1	
0920						CLK from Port5 to Port4	
1.Change U74,U21,U22 mos to 3*3 thermal pad package:SB00000GW00						5.Change mSATA SATA port from Port1 to Port0	
						6.Add USB port 12 for mSATA	
0921						7.Remove D11,D12 and C357,C358 (HDMI RF request)	
1.TB chip:U66 footprint add "-NH" for Non HDI					0929	8.C396,C324 change to 0201	
2.1.8p_0402:C402,C404 change to 75ohm_0402:R263,R264					1.Remove C510,C511	9.Remove C472 for +5VALW source cap	
					2.Remove Camera Choke:L7,R13,R14		
					3.Q1,Q2 change to DMN66D0LDW-7_SOT363-6:SB00000DH00	1014	
					4.R273,R394 change from 0_0603 to 0_0402	1.Remove DPST_PWM buffer:U13,R783,R85	
					5.Remove Step Motor SW1	2.Change +3VS_FULLL cap:C475,C466 from 0.1uF_0402 to 0201	
					6.Change LED/B connector from 8 pin to 4 pin	3.Change SATA cap:C621,C622,C623,C624 from 0.01uF_0402 to 0201	
					7.Change Jumper from 43*118 to 43*79		
					=>J2,J8,J10,J11		
0922							
1.Change C1457,C1505 form 1.8P 0402 to 0201:SE00000HB80					0930		
2.Del DDR CHA,B no use CLK1,CLK1# circuit					1.Remove +VCCSA cap:C1182,C1183	1017	
3.Change C606,C607 from D2 330uF to B2 330uF 2.5V ESR 15mohm:SGA00004400					2.Remove +USB3_VCCA cap:C390	1.Add power source of +VCCAFDI_VRM at P.20	
4.Swap total KB connector:JKB1 pin define					3.Change C427,C428 to 0.1U_0201_10V6K	2.Update DS3,AOAC control signal connected to EC	
					4.Add ESD diode:D6 for TP SMBUS		
					5.Change L65 to 220ohm 3A 0805	1018~1021	
					6.Swap DDR ChB Data,DQS# 6,7		
					7.Change U12 mos to 3*3 thermal pad package:SB00000GW00	1024	
0923						1.Remove R130	
1.Add DS3 function:SUSWARN#,SUSACK#,EC_DRAMRST_GATE					8.Remove X2,C1361,C1362	2.Define DRAM ID	
2.Add Motor function:Motor_IN1,Motor_IN2,Motor_IN3,Motor_IN4,					9.C378+C375 change to 10uF*1	3.Update TB schematic	
Door_Det_L,Button: KSI0 & KSO10					10.C460+C459 change to 10uF*1	4.Swap USB2.0 ESD pin	
3.Remove PCH NCTF test point					11.Remove C986,C987,C989,C990	5.Add on/off BTN for debug	
4.HDMI Fuse:F1 change to P5WS5 use footprint:F_1812					=>Add 1uF 0201*10		
5.Remove HDMI common mode choke:L36,L38,L39,L40						1027	
6.Change 0.1uF_0402_16V7K to 0.1uF_0201_10V6K:SE00000SV00					1003	1.Swap JTP1 pin for new module	
=>C521,C520,C526,C449,C523,C537,C541,C494,C495,C490,C497,C771,C522,C471,C473					1.Change EC side GPIO:PWR_LED to PWR_LED#,Remove Q32,R512	2.Gerber schematic	
7.Change 0.01uF_0402_16V7K to 0.01uF_0201_10V7K:SE172103K80					2.For separate coaxial and wire,update eDP MB connector pin define		
=>C425,C462					3.Remove JLED1 connector		
8.Change C751,C752 to B2 220uF 2.5V ESR 15mohm:SGA00004500					4.Change C427:0.1U_0402_16V4Z to 0.1U_0201_10V6K:SE00000VS00	1028	
						For Load BOM	
0924						1.Update Block Diagram	
1.Make MB to Audio/B connector pin define					1005	2.Update CPU,PCH part number	
2.Change RP 8.2K:R256,R262,R276,R386 to 8.2K_0402					1.Swap DDR ChB Data,DQS# 6,7	3.Update BOM config	
3.Change RP 10K:R386 to 10K_0402					2.Change PCH PCIE 0.1U_0402_16V7K to 0.1U_0201_10V6K:SE00000SV00		
4.Update TB schematic p.24,25,27					=>C572,C573,C617,C618,C681,C682,C683,C684,C685,C686,C687,C688	1101	
5.Change Q64,Q68 from AO3419L:SB000006R10 to AP2301GN-HF:SB000007H10					2.Change eDP cap from 0.1U_0402_16V7K to 0.1U_0201_10V6K:SE00000SV00	1.For整合料	
6.Integration of all 2N7002 SOT23 parts to SSM3K7002F_SC59-3:SB000009080					=>C910,C911,C912,C913,C914,C915	2.Combine PWR schematic	
=>Q74,Q20,Q1,Q2,Q32,Q16,Q17,Q14,Q37,Q7,Q21,Q23,Q24,Q5,Q34,Q29,Q60,Q66,Q67,Q72					3.Add R80:0ohm of H_CPU_PWRGD for ESD request	3.A test SMT schematic	
Not yet=>Q6,Q78,Q79					4.Remove On Board WLAN:MD225		
					5.Add Motor parts (Not Ready)		
0925					6.Add iSSD i100 parts (Not Ready)		
1.Delete LVDS function,Combine eDP,Card Reader function to JLVDS1							
Remove:R259,R260,R285,R286,R156,R157,TXCLK+,-,TX0+1,TX1+,-,TX2+,-,DDC CLK,DATA					1006		
Remove:C462,C425,C412,L20,only place PU:R271,R272,PD:R270,R280					1.Change R754,R751 0ohm from 0603 to 0402		
2.Change all SSM3K7002F_SC59-3:SB000009080 to SSM37K002FU_SC70-3:SB000009610					2.Change C484 0.1U from 0603 to 0402		
=>Q74,Q20,Q1,Q2,Q32,Q16,Q17,Q14,Q37,Q7,Q21,Q23,Q24,Q5,Q34,Q29,Q60,Q66,Q67,Q72					3.For DS3,Change power source from +3VALW_PCH to +VCCSUS3_3		
Not yet=>Q6,Q78,Q79					4.Change R629 from 0_0805 to 0_0402		
3.Change 10U_0805_6.3V6M:SE093106M80 to 10U_0603_6.3V6M:SE000005T80					5.Change SATA cap from 0.1U_0402_16V7K to 0.01U_0201_10V7K		
=>C754,C543,C418,C465					=>C621~C628		
4.Remove 0_0603_5%:R416,R421,R426,R327							
0926							
1.Change HDMI level shift Q16,Q17 to DMN66D0LDW-7_SOT363-6:SB00000DH00							
2.Modify TB schematic 0402 cap to 0201							
0927							
1.Remove J7					1010		
2.Change C599 330U D2 2V ESR 9mohm to 330U B2 2.5V ESR 15mohm:SGA00004400					1.Add BATT_RST#,VR_LEFT,VR_RIGHT pin		
3.Change EC +3VALW_EC					2.Add iSSD i100 128GB*2 schematic		
0.1U_0402_16V4Z to 0.1U_0201_10V6K:SE00000SV00					3.Add USB_HPD# pin		
=>C1198,C1199,C1200,C1201,C1204							
1000P_0402_50V7K to 1000P_0201_16V7K:SE000007U80							
=>C1202,C1203					1011		
4.Remove R329					1.Add Battery Reset function		
5.Change C751,C752 to 22U_0805_6.3V6M:SE000000I10					2.Swap USB2.0,3.0 choke for connector side 順線		
6.Remove J4(one of +1.05VS_VTT to +1.05VS_PCH jumper)							

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	EE P.I.R	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Revision	Document Number	Rev
				50	Q3ZMC M/B LA-8481P Schematic	1.0
				Date:	Thursday, April 12, 2012	Sheet 50 of 51

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/4/6	Deciphered Date	2013/4/6	Title	EE P.I.R	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 1.0	
				Q3ZMC M/B LA-8481P Schematic		
				Date	Thursday, April 12 2012	
				Sheet	51	of 51